zero. Therefore, the final result is
\[ f_{\text{max}} = \frac{1}{2 \Delta R} \]  

IV. DISCUSSION

The results of the analysis made in the previous sections were checked experimentally and with SPICE simulations. A junction-isolated 4-GHz Si-bipolar technology and an oxide-isolated 10-GHz Si-bipolar process were assumed for the computer simulations. The 4-GHz process resulted in a maximum frequency of operation of 115 MHz for the D-type master–slave version and 175 MHz for the R–S latch version. The 10-GHz process yielded a maximum frequency of 600 MHz for the D-type master–slave version and 770 MHz for the R–S latch version. The power dissipation was about 475 mW with a single 5-V supply. For the 4-GHz process, \( \Delta R \) is about 4 to 4.5 ns with the D-type master–slave flip-flops. From (12), these values give an estimated maximum frequency of 100 to 125 MHz, agreeing with the simulation results above. Similar estimations can be made for the other circuit and process combinations. They all agree closely with the SPICE simulations.

Measurements were performed on a commercially available R–S latch version of the circuit (MC 12040) which uses a 1-ns gate delay bipolar technology and consumes a power of 520 mW [5]. \( \Delta R \) measured from the phase characteristics was 5 ns. This puts the upper limit on the frequency of operation at 100 MHz, which is 20 MHz above the typical operating frequency of 80 MHz given in the data sheet.

In conclusion, simple and accurate analytical expressions have been derived for the phase- and frequency-acquisition characteristics of conventional DPFD’s. These equations clearly show the effect of the self-terminating feedback-path delay on the speed performance of the circuits.

REFERENCES


1. INTRODUCTION

Monolithic integrated charge-sensitive amplifiers have become widely used in high-energy physics and several charge readout amplifier systems have already been realized in CMOS technology [1]-[3]. However, the large 1/f noise and radiation sensitivity of the CMOS devices curtails the application range of these amplifier systems. Monolithic technologies that permit the integration of junction field-effect transistors (JFET’s) and MOSFET’s in the same process significantly widen this range. The JFET is a low-noise and intrinsically radiation-hard device and thus is highly useful in designs of low-noise amplifiers used in a high radiation environment [4].

II. THE JFET PROCESS

The n-well CMOS process available at the Fraunhofer Institute allows the integration of JFET’s without any modification of the underlying CMOS parameters [5]. Only one additional implant for the channel of the JFET is necessary (Fig. 1). The n-channel implant, which is situated in the p-substrate, determines the transistor parameters. The p+-gate is implanted together with the p+-diffusion of the PMOS transistors while the n-source and drain contacts are the same as the n+-diffusion areas of the NMOS transistors in this CMOS process. The back gate of this transistor is the substrate, which imposes restrictions on the use of this type of device.

The signal-to-noise ratio in the measurement of the charge delivered by a capacitive signal source is determined by the gain-bandwidth product \( g_m \)/\( C_i \) in the amplifier input device. As the back gate, compared to the top gate, provides a larger \( C_i \) and a smaller \( g_m \) contribution, it is advisable to tie the back gate to a fixed potential rather than connecting back and top gates together.

The noise characteristics of an n-channel JFET with gate width \( W = 400 \, \mu\text{m} \) and gate length \( L = 4 \, \mu\text{m} \), implemented in the process described above, are illustrated in Fig. 2. The spectral noise density of the JFET has been measured before and after exposure to a 1-Mrd dose of \( \gamma \)-rays from a \(^{60}\text{Co} \) source.
Power Supply Voltages
Power Dissipation
1.6 mW

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>NIFET-PMOS Preamplifier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltages</td>
<td>±5 V</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>1.6 mW</td>
</tr>
<tr>
<td>Rise Time</td>
<td>120 ns (Cg = 0 pF)</td>
</tr>
<tr>
<td></td>
<td>250 ns (Cg = 22 pF)</td>
</tr>
<tr>
<td>Open-Loop Voltage Gain</td>
<td>72 dB</td>
</tr>
<tr>
<td>Chip Area</td>
<td>0.0046 mm²</td>
</tr>
</tbody>
</table>

III. THE MONOLITHIC CHARGE-SENSITIVE PREAMPLIFIER

Investigations of noise performance and radiation hardness of JFET and CMOS devices, available in the technology described above, have served as the basis for the preamplifier design. Though the n-channel JFET has been found very useful for low-noise radiation-tolerant applications, there is still a need for a complementary transistor (to implement loading devices) and an enhancement transistor (to implement analog switches and digital components). Our investigations have shown that the noise of the PMOS devices is acceptable and its variation under irradiation is negligible [7]. Since they are of enhancement type, they can realize both loading and switching functions. Thus, no additional transistor types are required.

Using these two types of transistors we have built a switched-capacitor preamplifier for high-energy physics applications. The open-loop amplifier (Fig. 3) contains a folded cascode made of an NIFET (M1) in the common-source connection and a PMOS (M2) in the common-base configuration. The NIFET cascode (M1, M2, M3) provides the active load for the transistor M2. The switched-capacitor network consists of the feedback capacitor CF1, which is connected between the drain of M2 and the gate of M1. Charge reset on the feedback capacitor is activated by the PMOS switch MF1. The signal at the M2 drain is transmitted to the output buffer M1, M2, M3, M4, working at the same current density, will leave the output at nearly zero dc level during reset.

The measured data of this monolithic preamplifier are summarized in Table I (where Cg is the signal source capacitance), and the chip photomicrograph can be found in Fig. 4. Table II shows the device parameters and device currents of this preamplifier.

To investigate the effects of irradiation, the preamplifier was exposed to increasing dose levels of γ-rays from a 60Co source.
The spectral power density of the equivalent input noise is the noise spectra before irradiation and after 150-krd absorbed dose. At this level of absorbed radiation dose no change of the dc parameters has been seen. Measurements with higher doses are affected by ionizing radiation as shown in Fig. 5, which contains only a small increase of noise after irradiation.

The spectral power density of the equivalent input noise is affected by ionizing radiation as shown in Fig. 5, which contains the noise spectra before irradiation and after 150-krd absorbed dose (curves a and b, respectively).

According to Fig. 4 the absorbed dose did not affect the noise spectrum in the frequency region above 1 kHz. Only at lower frequencies is there a small increase of noise after irradiation. At this level of absorbed radiation dose no change of the dc parameters has been seen. Measurements with higher doses are planned in the near future.

IV. SUMMARY

The preamplifier we have presented in this paper shows the advantages which can be expected from a JFET-MOS circuit: low-noise and radiation-tolerant behavior. It uses a JFET fully compatible with the standard CMOS technology available at the Fraunhofer Institute. This JFET requires only a simple modification of the standard process: one implantation for the channel of the JFET. Using this process extension we can combine the analog and digital switching and storage.

As the irradiation shifts the threshold voltage of NMOS devices towards depletion, they are not of great use for analog switching. This has to be taken into account when implementing radiation-hardened digital circuits. Appropriate substrate bias and channel stoppers might be necessary to adjust the threshold voltage of NMOS devices and reduce leakage currents. The essential conclusion of the contribution is, however, that the design of radiation-tolerant analog circuits in a standard CMOS technology is feasible. Our contribution has demonstrated that a preamplifier based upon JFET-PMOS design exhibits excellent noise performance and is virtually unaffected by exposure to γ-rays up to a total absorbed dose of 150 krd. The feasibility of analog switching indicates a possible extension towards the realization of other circuits, e.g., A/D and D/A converters, switched-capacitor filters, etc., for high radiation environments.

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REFERENCES


Active Compensation of Operational Transconductance Amplifier Filters Using Partial Positive Feedback

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Abstract—An active compensation technique to improve high-frequency performance in OTA-C filters is presented. Each critical OTA is replaced by two OTA's connected in parallel with opposite polarity and with different transconductances. The novel feature of this technique is that it does not require tuning to reduce excess phase and yields filters with extended tuning range. It is demonstrated by a programmable bandpass filter from 1 to 9 MHz fabricated in 3-μm CMOS technology.

I. INTRODUCTION

In this paper we propose a novel scheme for active compensation of OTA-C filters [1]–[4] that has two very attractive features. 1) It does not require tuning of the compensating element.