Abstract—The detailed study of random telegraph signal (RTS) currents and low-frequency (LF) noise in semiconductor devices in recent years has confirmed their cause and effect relationship. In this paper we describe the physical mechanisms responsible for RTS currents in any device. The methods for calculating the amplitudes and characteristic times of the RTS currents produced by traps with known electrical characteristics and locations are described. The noise spectra in junction field effect transistors (JFET’s) resulting from traps in the silicon or the oxide are derived as a function of basic device parameters, operating conditions and temperature. Experimental results verifying the predictions of the models are presented.

I. INTRODUCTION

The physical origins of excess LF noise in JFET’s were attributed to variations in channel carrier density due to fluctuations in occupancy of generation-recombination (GR) centers in the channel by van der Ziel [1], while Sah [2] and Lauritzen [3] said that the dominant centers were in the depletion region and modulated the channel by field effect. The theory of Sah and Lauritzen was proved experimentally with gold doped devices operating around room temperature.

Recent theories of LF noise state that the number of carriers and/or the carrier mobility have random fluctuations in the conducting region caused by traps and express the LF noise as a function of the total number of carriers in the device using the Hooge equation [4] as the starting point. Attempts have been made to apply this method to the whole class of active electronic devices [5]. In these empirical formulae it is assumed that the noise has a 1/f spectrum. An arbitrary factor [6] is needed to fit the theory to the measured values for each device and operating condition. The description of the underlying physical mechanisms responsible for the fluctuations has often taken second place to the fitting exercise. The numerous papers and conferences on the subject have increased the variations in these theories without a consensus on a preferred model.

An important development was the observation of bistable current waveforms resembling random telegraph signals, originally called burst noise but now commonly referred to as RTS currents, first discovered in the early 1950’s [7]. In the past three decades there have been numerous reports of such phenomena in a wide range of semiconductor devices. Card and Chaudhari [8] and Wolf and Holler [9] found burst noise in reverse biased emitter-base junctions of bipolar transistors. Burst noise in bipolar transistors were reported by Giralt et al. [10] and studied in detail by Blasquez [11] who analyzed the characteristic as a function of bias and temperature. Knott [12] found unusual intermittent forms of burst noise in bipolar transistors. RTS currents in junction field effect transistors (JFET’s) were reported by Kandiah et al. [13] who proved that they were generated by charge transitions at single point defects (traps) in the Si and that the LF noise in JFET’s was mainly due to the RTS currents [14]. RTS currents in metal-oxide-semiconductor field effect transistors (MOSFET’s) were reported by Ralls et al. [15] and Uren et al. [16]. Kirton and Uren [17] reviewed the theory and experimental data on RTS currents in microstructures.

The proven correlation between the occurrence of RTS drain currents and LF noise [11]–[17] gives strong support for the McWhorter model [18] for noise in inversion mode MOSFET’s, sometimes called the number fluctuation model. This paper is a review of the model for RTS currents due to traps in semiconductor devices from first principles fully described elsewhere [19] using an adaptation of Ramo’s theorem [20] and an introduction to a model for LF noise resulting from RTS currents. The model can be used to derive explicit expressions for RTS currents and LF noise in any device but this paper is largely confined to silicon JFET’s. We obtain the total noise power spectrum due to traps from the summation of the noise due to the RTS currents of individual traps.

Established physical principles are used with the following exceptions:

1) adapting Ramo’s theorem to obtain the amplitude of the RTS current due to charge trapping or release,

2) defining the effective carrier density near an interface with the oxide [19] and,

3) defining a coupling factor between a trap site and the channel of a field effect transistor (FET).

We have assigned values to some parameters when they are not known or cannot be ascertained experimentally such as trap locations or densities in order to compare theoretical predictions with measured values.

RTS currents occur in all doped semiconductor devices since even the dopant atoms generate them. However RTS currents are only rarely observed in a few classes of devices and only under very limited range of operating conditions. The physical
models outlined in this paper can explain these apparently conflicting statements.

II. SOME EXPERIMENTAL RESULTS

In this section we report on measurements of the temperature and bias dependence of noise in JFET's and MOSFET's as an introduction to the development of our model. We find that all published results and our extensive measurements of amplitudes and mean times of RTS currents and of LF noise are within the range of values predicted by our model.

A. LF noise in JFET's and MOSFET's

Increases in the noise of JFET's at low temperatures were reported by Radeka [21], Klassen and Robinson [22], and Haslett and Kendall [23]. These and more recent publications showed that the noise behavior of JFET's could be summed up as follows:

1) Thermal noise at moderately high frequencies steadily decreases as the temperature is reduced below room temperature down to a critical temperature.
2) Below the critical temperature the thermal noise increases sharply. The critical temperature is a function of device doping, geometry and operating conditions [24].
3) There are excess LF noise components which show groups of peaks as a function of temperature [14], [23] over the entire range of useful values. The positions of the peaks in any one group goes to lower temperatures at lower frequencies. The magnitudes of the peaks are often very strong functions of bias conditions [13], [14].
4) There is often a $1/f$ component which is independent of temperature but weakly dependent on bias.

These characteristics are illustrated in Fig. 1 which shows the noise at 8 frequencies of a low noise JFET type 5165A, with a $140 \times 4\mu$m gate, as a function of temperature. In most JFET's, with larger gate areas or higher defect densities, the characteristics are more complicated than those shown in Fig. 1. These results were selected because they show the four distinctly identifiable components mentioned above. At frequencies in excess of 100 kHz the thermal noise varies with temperature as described above with a critical temperature of about 150 K. Between 120 K and 250 K there is a $1/f^2$ component which is a very strong function of temperature with a group of peaks which will be discussed in Section V. In general there are other groups of peaks at lower or higher temperatures than that in Fig. 1. There is a $1/f$ component which is particularly noticeable above 250 K although this component is present at all temperatures.

The most significant measurements which showed that the source of LF noise in small devices is strongly localized were those of LF noise as a function of channel position in 4-terminal JFET's. In these devices the shape of the conducting channel will not change significantly if the drain current and voltage are held constant while the relative gate/substrate bias is changed. The gate/substrate bias will effectively move the channel in a direction normal to the substrate. A typical result in Fig. 2 shows the noise at three frequencies as a function of substrate bias, with the gate bias adjusted to maintain constant drain current, in the 4-terminal JFET type PSO1, with a $400 \times 4\mu$m gate. The temperature for the measurement at each frequency was chosen to be that which gave the highest noise. The significance of the appearance of peaks, their number over the maximum useful bias range and positions as a function of frequency will be discussed in Section IV.

Most measurements of the gate referred LF noise on inversion mode MOSFET's with gate areas greater than a few $\mu$m$^2$ show that the noise power has a $1/f$ spectrum and is

1) inversely proportion to gate area,
2) proportional to the oxide thickness,
3) almost independent of temperature in the range 80 K to 350 K,
which showed that nearly all the LF noise was generated by traps in the Debye region adjacent to the channel. It was later developed [25] to explain the results of our measurements on inversion mode MOSFET’s. More recent developments of the model [26] identify the physical origins of the $1/f$ and $1/f^2$ components of noise in depletion mode MOSFET’s.

The characteristics of an RTS current are the amplitude and the mean times in each of the two states. The mean times are derived by using well known methods in Sections III-A and III-B. The model for amplitudes is outlined in Section III-C.

The analysis of RTS currents and LF noise in MOSFET’s will be published elsewhere. However we shall summarize the effects due to traps in oxides close to the interface with the semiconductor since our results show that RTS currents and excess noise in the gate and $1/f$ noise in the drain current of a JFET are generated by spurious MOSFET’s found in all JFET’s.

A. Mean RTS Times for a Trap in a Semiconductor

It is assumed that the trap has only two charge states with the more negative state being designated state 0 and the other as state 1. The distribution of the times in each state is exponential. In general each transition can take place either by the capture of one type of carrier or the emission of the opposite type of carrier. If there are two competing processes with mean times $\tau_a$ and $\tau_b$ for the same transition then the effective characteristic time $\tau$ is given by

$$\frac{1}{\tau} = \frac{1}{\tau_a} + \frac{1}{\tau_b}. \quad (1)$$

In most situations one route will dominate each transition but some important exceptions will be discussed later.

We shall not discuss the rarer types of traps which have multiple charge states or concern ourselves with the details of the transition process except to assume that it takes place in a very short time. Simultaneous trapping of many carriers is not considered.

The mean times $\tau_c$ for capture and $\tau_e$ for emission are given by

$$\tau_c = \frac{1}{n\nu_T \sigma} \quad (2)$$

where $n$ is the density of free carriers around the trap, $\nu_T$ is the thermal velocity of the carriers, $\sigma$ is the capture cross section and $\tau_e = \exp(E_e/kT)/GN_e \nu_T \sigma \quad (3)$

where $E_e$ is the energy level of the trap relative to the band edge, $k$ is Boltzmann’s constant, $T$ is the temperature, $G$ is a degeneracy factor with a value between 1 and 4, and $N_e$ is the density of states at the band edge. The appropriate band edge is used for electrons or holes.

The appearance of a capture cross section in the emission time in (3) is a result of the assumption that the transitions of charge state at a trap normally occur by alternate capture and emission of the same type of carrier. In a number of situations this is not true. There are also other minor complications relating to donor type traps in the lower half of the bandgap or acceptor type traps in the upper half of the bandgap which cannot be dealt with adequately in this paper.

B. RTS Current Waveforms

In both JFET’s 5165A and PS01 we observed clear RTS drain currents with amplitudes ranging from less than 0.5 nA up to 4 nA and mean times in each of the two states ranging from less than 100 $\mu$s to over 100 ms, depending on the bias and the temperature in the range 100 K to 180 K, when operated under conditions close to or within noise peaks.

Fig. 3 shows the waveforms of the gate current of a JFET with 100 x $4\mu$m gate and the drain current of a depletion mode MOSFET with a 100 x $6\mu$m gate. The drain current in a depletion mode MOSFET has the same noise characteristics as a JFET when bulk traps are present in the silicon. These results cover only part of the range of our observations of amplitudes and mean times of RTS currents. The full range extends in amplitudes from a few fA to 20 nA, and in mean times from 100 $\mu$s to many days. Both waveforms in Fig. 3 show the presence of at least two independent RTS currents and only a fraction of the recordings show the characteristics of a single random telegraph signal. Extremly good control of parameters is essential for making quantitative measurements on RTS currents and great care is also necessary to specify all the operating conditions for comparison with theoretical predictions especially for MOSFET’s.

III. THE MODEL FOR RTS CURRENTS AND LF NOISE

This model was initially formulated to explain the observed characteristics of RTS currents and the associated LF noise in 4-terminal silicon JFET’s with small gate areas [13], [14]...
B. Mean Times for Traps in an Insulator Close to an Interface with a Semiconductor

The charge exchange between a trap in the oxide and carriers in the neighboring semiconductor region is through the Fowler-Nordheim tunnelling process. The mean time $\tau_i$ is given by

$$\tau_i = \exp(2Kz)/4\nu_0\sigma$$

where

$$K = \sqrt{2mE_0/h}$$

$z$ is the distance from the trap to the interface, $n$ is the density of carriers in the semiconductor region adjacent to the trap, $m$ is the effective mass of the carrier, $E_0$ is the barrier height at the interface and $h$ is the reduced Planck's constant.

The value of $n$ in (4) is indeterminate because:

1) The carriers do not have an omnidirectional uniform distribution of thermal velocities on the semiconductor side of the interface.

2) The carrier density has a very complex distribution for distances of a few nm from the interface [27] which is not correctly given by the classical description.

In our model [19] we take $n$ to be the average carrier density over a Debye length $L_D$ into the semiconductor from the interface since it determines the attempt rate of carriers in the semiconductor to overcome the potential barrier at the oxide. The precise value of $n$ is however not critical in evaluating the LF noise due to oxide traps in many situations as will be demonstrated in the full analysis to be published elsewhere.

C. RTS Amplitudes

Ramo's theorem states that the current induced into an electrode by a carrier moving in its field is given by

$$\Delta I = quE_u$$

where $q$ is the electronic charge, $u$ is the instantaneous velocity of the carrier and $E_u$ is the component of the incremental electric field per volt in the direction of $u$ due to that electrode at the point occupied by the charge. The application of this theorem and Poisson's equation to the two situations at and around a trap before and after the capture or release of a carrier yields the result that the current in the electrode will change around a trap before and after the capture or release of a carrier.

Let us consider a trap in a semiconductor filament with a uniform cross section and length $L$ with a voltage $V_0$ applied across it. From (6) the amplitude of the RTS current due to a carrier moving in its field is given by

$$\Delta I = qu/L$$

If we write $u = \mu V_0/L$ where $\mu$ is the mobility we obtain

$$\Delta I = quV_0/L^2$$

which is the formula quoted by McWhorter [18]. It is seen that the amplitude of the RTS current generated by a trap in this filament is independent of the position of the trap. In practice this would not apply to trap positions near the surface since the mobility there will be lower than that deeper in the semiconductor. There will be a spatial variation of the amplitude as a function of the position at right angles to the field.

It has been shown [28] that (7) also applies to the case of a trap close to the channel of a field effect transistor with a channel length $L$.

D. LF Noise Spectra

Following Machulup [29], an RTS current with an amplitude $\Delta I$ and mean times $\tau_0$ and $\tau_1$ in the two states has a Lorentzian spectrum with a cutoff frequency $f_c$ given by

$$f_c = \frac{\tau_0 + \tau_1}{2\pi\tau_0\tau_1}$$

and a power density at very low frequencies given by

$$i_{n0}^2 = \frac{(2\Delta I\tau_0\tau_1)^2}{(\tau_0 + \tau_1)^3}.$$  

The power spectral density of the noise due to a trap is

$$S(f) = \frac{i_{n0}^2}{(1 + (f/f_c)^2)}.$$  

The mean times in the two states are usually independent. If one has a fixed value and the other is variable the noise $i_{n0}$ at low frequencies will be maximum, for a fixed $\Delta I$, when

$$\tau_1 = 2\tau_0.$$  

This relationship is important in understanding the characteristics of peaks such as those in Fig. 1 and Fig. 2.

The procedures for calculating the total LF noise in any device for specified bias conditions, as described in earlier papers [14], [25], [26] are as follows:

1) Calculate the RTS amplitudes and mean times of every trap in the device.

2) Derive the RTS amplitudes and mean times of every trap in the device.

3) Sum the power spectra for all traps.

E. General Comments

JFET's show very large scatter in the gate referred LF noise as a function of bias and temperature even in devices from the same manufacturing batch but, in our experience, inversion mode MOSFET's show very little dependence on any parameters. Yet there is greater controversy on the origins and modeling of RTS currents and noise in inversion mode MOSFET's. Kirton and Uren [17] have discussed the very wide range of mean times and amplitudes of RTS currents that have been observed in MOSFET's and the difficulty in interpreting the effects of bias and temperature on these parameters.

The wide range in RTS characteristics and LF noise levels are due primarily to two important factors. The first is the dependence of the RTS amplitude, from (6), on $u$ and $E_u$. Extremes in the values of these two parameters are found in the following simple examples:

1) Values of $u$ at the source and drain of a FET with a gate length of 1 µm with only 1V on the drain.
2) Values of $u$ and $E_u$ at different locations in the base emitter junction of a bipolar transistor.

The dependence of the characteristic times on the values of $n, T, E_u, \sigma$, and $z$ pertaining to the trap and its location will result in a wide range of values for these times. The variations in amplitudes and mean times of RTS currents inevitably result in large scatter in the LF noise in small area JFET's. The reasons for the nearly complete independence of the gate referred LF noise in MOSFET's on these factors will be described elsewhere.

The obvious difficulties in validating the model are that we cannot determine the characteristics of a particular trap or its location in a device by an independent method nor place a trap with known characteristics experimentally in a specified location and measure the consequential changes.

IV. ANALYSIS OF SOME SITUATIONS IN JFET'S

In the following sections we calculate the effects of individual traps with arbitrarily chosen parameters at various locations in the active regions of a JFET and compare these with corresponding measurements.

A. RTS Amplitudes

Let us apply the expressions for RTS amplitudes given in Section III-C to a JFET with the following assumptions:

1) The channel is long.
2) Below drain pinch-off the carrier mobility in the channel is constant.
3) Above drain pinch-off the field increases sharply for a short length near the drain, which we shall call the pinched-down region.
4) At high drain voltage the carrier velocity at the drain is the thermal velocity.

There is inadequate space to give a rigorous treatment to the extension of Deighton’s derivation of RTS amplitudes [28] to traps within the channel of a FET but we shall assume the validity of (7) throughout the channel and its bounding regions.

The RTS amplitude will increase progressively as a function of the trap position from the source to the drain with the fastest rate of change for traps in the pinched down region. The amplitude for a trap in this region has an absolute maximum value when $u = u_t$. From (7) we expect this maximum amplitude of RTS current in a JFET with a channel length of $4\mu m$, typical of many of the JFET's used in our studies, to be $4 nA$ at room temperature.

For a uniform density of defects we would expect, from the assumption 2) above, an almost equal probability of every amplitude from small values to $4 nA$ at pinch-off. We should not see any amplitudes in excess of $4 nA$.

Our measurements on JFET's and MOSFET's, with values of $L$ ranging from 1 to 5 $\mu m$, from below pinch-off to well above pinch-off, are in agreement with these expectations.

Since the drift velocity of carriers in the Debye region next to the neutral channel will be the same as those in the adjoining neutral channel region we shall assume that (7) also applies to traps in the Debye region.

Equation (7) applies also to traps located a short distance inside the oxide adjacent to the channel of a MOSFET in strong inversion. The distance is assumed to be small compared to the Debye length within the semiconductor and to the oxide thickness.

B. Traps in Neutral Channel Region

1) Let us, for example, consider a donor type trap with a capture cross section of $10^{-15} cm^2$ in the neutral channel region of an n-channel JFET. Assuming a channel doping density of $10^{16} cm^{-3}$ the mean time $\tau_n$ in the ionized state (i.e., the capture time) of the trap will be less than 10 ns at any temperature above 80 K. RTS currents with such short dwell times will not be observed irrespective of the time in the other state. From (10) and (11) we find that the power spectral densities of the resulting noise will not be as significant as suggested by van der Ziel [1] except for very shallow traps or traps with a very small capture cross section.

An interesting exercise is to consider the dopant itself as a trap. If its energy level is 0.05 eV below the conduction band and the capture cross section is $10^{-15} cm^2$ the values of $\tau_n$ and $\tau_i$ at 77 K for the above doping level will be about 13 ns and 29 ns, respectively, so that there will be nearly symmetrical RTS currents. There will be $10^7$ dopants producing such RTS currents in a JFET with a channel volume of $1000 \mu m^3$ but only a small fraction of dopants at the drain end of the channel will generate large amplitudes. These RTS currents will generate noise with a flat spectrum up to a frequency of about 17 MHz, which is the situation predicted by van der Ziel [1]. Another interpretation of this effect, according to Churchill and Lauritzen [30], is that at 77 K there will be carrier freeze out of about 30% accompanied by an increase in total noise.

Our model directly calculates the carrier freeze-out fraction and the excess noise due to carrier freeze out. The model predicts that there will be a $f^{-2}$ rate of fall-off at frequencies above 17 MHz until it reaches the level of the Johnson noise. We have observed that the noise at low frequencies increases typically by a factor 10 over Johnson noise as the temperature is reduced from 150 K to 77 K as predicted by the model.

C. Traps in the Debye Region

It will be shown in this section that the traps in the Debye regions on either side of the channel make the most significant contributions to RTS currents and LF noise in JFET's due to traps with any characteristics, except those with energy levels very near midband which will be discussed in Section IV-D.

The most important aspect of RTS currents due to traps in the Debye region is the wide range of capture times due to the variation of carrier density as a function of distance normal to the channel. Fig. 4 shows the carrier density as a function of distance from the channel starting from an arbitrary point in the Debye region, as derived by Deighton [31]. Fig. 4 also shows the results of a simulation, using the model described in Section III, of the noise due to a trap in the Debye region at the drain end of the channel in a JFET identical to PS01 at the three frequencies and associated temperatures used in Fig. 2. The trap parameters for the simulation were obtained...
after more detailed measurements on the JFET type PS01 and comparing them with the model. Fig. 4 predicts the decrease in the height of the noise peak and the movement of the peak towards the neutral channel region at the higher frequencies, as seen in Fig. 2.

The following points emerge from the comparisons:
1) The positions of the associated noise peaks in Fig. 2 at the three frequencies due to traps A and B as a function of substrate bias, for constant drain current, indicates that these traps lie in the Debye region on the far side of the channel from the substrate, confirmed by the form of the slight asymmetry of the peaks.

2) Comparing Fig. 2 and Fig. 4 it appears that a substrate bias change of about 0.6 V moves the channel by 1.2 \( L_D \). This is consistent with the doping density of the channel and the gate bias voltages for maximum noise from trap A.

3) The simulation does not include the thermal noise of the channel or the \( 1/f \) component present in Fig. 2.

4) There are at least seven traps which have been swept through the Debye regions of the channel for the full substrate range in Fig. 2.

The traps responsible for the noise in Fig. 2 have an energy level of about 0.32 eV below the conduction band with a capture cross section of about \( 1.5 \times 10^{-15} \text{ cm}^2 \). Traps with these characteristics as well as another type with an energy level of about 0.17 eV from the conduction band with a larger capture cross section are found in most n-channel JFET's.

Hiatt et al. [32] found two types of GR centers (traps) with energy levels of 0.17–0.19 eV and 0.34–0.36 eV. These are probably the same types as those we have found. However Hiatt et al. follow van der Ziel's assumption [1] that the traps generate the noise only when they are present in a small part of the Debye region. The difference between these views has considerable significance when relating the magnitude of the total noise to the density of the traps.

An interesting example of the drain current noise due to a trap in JFET type XX51 with a \( 400 \times 4 \mu \text{m} \) gate, at very low temperatures, in which the channel position relative to the trap for constant drain current can be moved by the substrate bias over a very wide range is seen in Fig. 5. The temperature of 80.3 K in Fig. 5(a) gave the maximum noise at 10 Hz at the optimum substrate bias. The temperature of 97 K in Fig. 5(b) is the lowest temperature at which all the sharp peaks when the trap is in the Debye region, such as those in Fig. 5(a), disappeared. All the characteristics in this series of measurements, consisting of 8000 readings with a standard deviation of better than 2%, are entirely consistent with our model and show many important features predicted by the model.
Moving the trap to the following five different regions by the substrate bias voltage:

1) Bias > -0.2 V, in depletion region above the channel,
2) -0.2 V > bias > -1.0 V, in Debye region DB1 above the channel,
3) -1.0 V > bias > -2.0 V, in neutral channel region N.
4) -2.0 V > bias > -2.8 V, in Debye region DB2 below the channel.
5) bias < -2.8 V, in depletion region below channel.

The characteristics in Fig. 5 also show the following minor inconsistencies:

1) The magnitudes of the noise peaks at 10Hz at 80.3 K in regions DB1 and DB2 would lead to the conclusion that the trap is in the Debye region close to the drain, from Section III using the thermal velocity at 80.3 K.
2) The flat portions in the center in Fig. 5(b) indicate that the carrier density around the trap is constant for a bias change from -1.0 V to -2.0 V. The constant carrier density over such a distance is not consistent with a pinched-down region, at higher temperatures.
3) There are also major discrepancies between the energy levels and capture cross sections for this trap which we calculated from the complete noise measurements and the known characteristics of the Oxygen A-center which is usually identified with the traps observable in this temperature range.

D. Traps in the Depletion Region

Sah [2] and Lauritzen proved that LF noise in JFET’s operated near room temperature is generated by traps in the depletion region of the JFET with an energy level near midband. They calculated the total noise at a fixed temperature as a function of the trap density and the average fraction of the traps in one charge state. The assumption was made that the charge state transitions occur only by alternate emission of electrons and holes by the traps. According to our model, these calculations will give the correct noise level only if the depths of the depletion regions on both sides of the channel are much greater than a few $L_D$, for trap energies very close to midband and if the temperature is high enough.

Although our model does not impose the above restrictions there is a problem in applying (7) to a trap situated a long way outside the channel. This can be overcome if we introduce a charge coupling or mirror charge factor $M$ between the trap and the channel to express the field effect modulation of the drain current in (7). This factor is defined as

$$M = \frac{C_{ch}}{C_{tot}}$$

where $C_{ch}$ is the capacitance of the trap to the channel and $C_{tot}$ is the total capacitance of the trap. Thus a trap in a depleted region between the channel and the gate will have a value

$$M = \frac{D - d}{D}$$

where $D$ is the depletion depth and $d$ is the distance from the trap to the channel. This will be accurate only when the channel length $L$ is much greater than $D$.

Fig. 6 shows the noise in the n-channel JFET type PS4-52 as a function of substrate bias, at the same frequencies as in Fig. 5, at room temperature. The interpretation of these results from our model are:

1) The peaks occur when the trap is in the Debye region and the transition from state 1 to state 0 can occur either by capturing an electron or emitting a hole.
2) To the right of the peak in Fig. 6 the trap is in the depletion region where the electron capture has nearly zero probability.
3) Since the long tail occurs at substrate bias values higher than at the peak we conclude that the trap is on the same side of the channel as the substrate.

The theories of Sah [2] and Lauritzen [3] calculate the LF noise in the long tail in Fig. 6 assuming that capture rates are negligible. This can result in underestimates, for a given trap density, as the energy level moves even a few MeV away from midband or the temperature is reduced. The critical effect of the energy level on the noise distribution as a function of position of the trap is seen in the simulation in Fig. 7. It shows the noise in a JFET with the same gate and doping parameters as PS4-52, at the same frequencies as Fig. 6, as a function of distance of the trap from an arbitrary point in the Debye region for energy levels of 0.54 eV and 0.51 eV from the conduction band.

V. TOTAL NOISE IN A JFET

A. Trap Density in the Silicon

So far we have discussed the RTS currents and noise due primarily to one trap with arbitrary characteristics present at any point in the device as a function of temperature. The noise spectrum generated by each trap is simply Lorentzian with the drain current noise given by (11). We now address the
problem of the total noise in the JFET due to an arbitrary density of traps.

In Section IV we have seen that, except for traps with an energy level very close to midband, the contribution of any trap to LF noise rises steeply as the trap position moves towards the drain and into a critical range within the Debye region adjacent to the channel. Midband traps are not very important since material with a low density of such traps is more readily available as a result of recent developments for high performance charge coupled devices. From considerations of the practical usefulness of the device as an amplifier we need only consider conditions near or above drain pinch-off although our model fully describes conditions below pinch-off equally well.

Traps from the pinched down region up to a short distance $L_X$ in the direction of the source make the main contributions to LF noise owing to the effect of the carrier velocity in (7). The effective volume contributing to the noise, for a fixed operating condition, is therefore approximately equal to $W L_X F L_D$ where $W$ is the channel width, $L_D$ is the Debye length, and $F$ is a factor which we estimate to be about 10 from Fig. 4. $L_X$ is a small fraction of the channel length which increases slowly with increasing drain voltage. Although $L_X$ will be a larger fraction of the channel length for very small drain voltages we will ignore this as being unimportant. If the trap density is $10^{13}$ cm$^{-3}$ then there will be only 10 active traps, on average, in a device with $W = 1000$ $\mu$m, $L_X = 1$ $\mu$m, $F L_D = 0.1$ $\mu$m which has an effective volume of $100$ $\mu$m$^3$. We have decided that there would be little point in attempting to derive an accurate expression for the spectrum of LF noise in devices of this size or smaller for low trap densities since there would be large statistical fluctuations from device to device. Deighton has shown [33] that the spectrum of the noise in a JFET at very high trap densities (in excess of $10^{13}$ cm$^{-3}$ in the above example) has approximately a $f^{-1.2}$ fall off above the cutoff frequency given by (9) for any one type of trap.

It is possible to get a realistic estimate of trap densities in a JFET by counting the number of peaks in the results such as Fig. 2 if the measurements are carried out at very low drain currents (near gate pinch-off conditions) with a moderately high drain voltage. The effective volume swept by changing the substrate will then be almost equal to $W L_X T$ where $T$ is the total thickness of the available channel region. In the JFET type PS01 of Fig. 2 we estimate the defect density to be no greater than $5 \times 10^{10}$ cm$^{-2}$.

B. Comparing the Characteristics in Fig. 1 with the Model

Let us now look at the characteristics of the JFET type 5165A in Fig. 1 in some detail. The features in the temperature range 120 K to 250 K are consistent with the following conclusions:

1) the noise is generated by a single trap, based on additional measurements of the noise peaks as a function of gate bias,
2) the trap has an energy level of about 0.32 eV and capture cross section of $2 \times 10^{-15}$ cm$^2$ calculated from the dependence of peak temperatures on frequency,
3) it is located in the Debye region near the drain of the JFET from the absolute magnitudes of the noise at the peaks.

There are two other significant components of excess noise in Fig. 1. The first is the increased noise at temperatures below 150 K due to carrier freeze out which has been modeled as described in Section IV-B.

The second component which has a 1/f spectrum is clearly identified in Fig. 1, especially at temperatures above 250 K, by its virtual independence on temperature. We believe that this is generated by traps in the oxide near the edges of the gate and drain as shown in Fig. 8. Assuming that $\tau = \tau_1 = \tau$ in the expressions in Section III-D where $\tau$ is the tunnelling time given by (4) it can be shown that the drain current noise due to traps in unit area of oxide at $x, y$ for all values of $z$ is

$$S_i(f) = \frac{(M(x) \Delta I)^2 N_t}{8K f}$$  (15)

where $M(x)$ is the coupling factor in (14), $M(x) = x/D$ for the traps in this elemental volume, $\Delta I$ is given by (7) assuming that the carrier drift velocity is that at the drain end of the pinched down region and $N_t$ is the volumetric density of traps in the oxide. Integrating over all values of $x$ and $y$ we obtain the total spectral density of the noise due to the oxide traps referred to the gate

$$S_v(f) = \frac{W N_t x^2 y^2 \omega_d^2}{24K L^3 D^3 y_m f}$$  (16)

Fig. 7. Simulation of noise due to a trap near midband in a JFET similar to PS4-52 as a function of trap position, showing the critical effect of energy level on the noise when trap is in the depletion region at room temperature.

Fig. 8. Cross section of the region between the gate and drain in a JFET.
Fig. 9. Simulation of total noise in a JFET similar to 5165A of Fig. 1 under similar conditions.

A simulation of the noise in a JFET with parameters identical to type 5165A, whose characteristics are shown in Fig. 1, using our model is shown in Fig. 9. The parameters used in the simulation are:

1) \( W = 140 \, \mu m \), \( L = 4 \, \mu m \),
2) channel doping \( 10^{16} \text{cm}^{-3} \),
3) depletion depths of 0.3 \( \mu m \) at the source end and 0.6 \( \mu m \) at the drain end of the channel,
4) one trap with an energy level of 0.32 eV and capture cross section of \( 10^{-15} \text{cm}^2 \) in the Debye region near the drain, and
5) \( x_m = 200 \, \AA, N_t = 10^{17} \text{cm}^{-3} \).

The accuracy of the model is evident by comparing Fig. 1 with Fig. 9. The simulation slightly underestimates the increase in noise due to carrier freeze-out which is probably due to incorrect values of energy level or capture cross section of the dopant. The overestimate of the thermal noise at all temperatures and the small error in the \( 1/f \) component at very low temperatures is probably due to wrong assumptions for the temperature dependence of the transconductance.

C. Some Observations on RTS Currents in Fig. 3(a)

Fig. 3(a) is significant since it shows RTS currents of very small amplitudes with very long characteristic times in the gate current of a JFET. Long mean times are associated with low carrier densities (low currents). Our studies of JFET gate currents in 1981 suggested that they were not in the same category as the drain current RTS waveforms in JFET's we had been studying previously [13] since the characteristic times were well outside permissible values for midband traps in the silicon at room temperature. We concluded that traps in the oxide were responsible for these RTS currents which was confirmed by subsequent investigations of RTS currents and noise in small area MOSFET's. As discussed in Section V-B above, the regions between the gate and drain as well as between gate and source behave like MOSFET's for conduction current as well as for RTS currents, especially when taking into consideration the effects of connecting leads to these electrodes. This will be treated in detail elsewhere.

VI. CONCLUSIONS

We have shown that RTS currents due to a trap can be described analytically if the trap characteristics and its location are known. The LF noise due to traps can be calculated from the trap characteristics and locations if the device geometry is known.

It has been demonstrated that the observed characteristics of RTS currents and LF noise in JFET's due to traps in the silicon and in the oxide are accurately depicted by the model presented here. The variations of the characteristics with bias, temperature and device parameters follow the predictions of the model. It has also been shown that the model can give a good indication of where a particular trap is situated in relation to the channel and the density of traps if 4-terminal JFET's are available.

The situations analyzed in this paper are particularly relevant to devices with low trap densities. The complete noise spectrum in the presence of a high density of defects has not been discussed since small low noise JFET's will only have a few active traps generating significant levels of noise.

The models described by many authors often describe only part of the situation owing to the incomplete analysis of the conditions for charge state at traps in general and a lack of precise expressions for the effects of traps.

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