THE ELECTRONICS for CUORE

UCLA (testing)  
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USC (production)  
Frank T. Avignone, Ray Edmonds, Carl Rosenfeld, Kevin Wilson.

INFN-MIB (design, prototyping and validation)  
Andrea Giachero, Claudio Gotti, Gianluigi Pessina.  
Antonio Delucia  
Alessandro Baù (partial), Andrea Passerini (partial).
Links to the detectors: PEN and glue Kapton boards.

Detector

Very front-end (on the fridge)

Antialiasing

Bessel Filter

Small Faraday Cages

Close to the DAQ

DAQ

Power supply system

Linear Supply, ±9 V, ±5 V

DC/DC 48 V to 12/6 V

48 V AC/DC

K = Kapton

= PEN

= Constantan

Heater Pulser

Calibration Pulse Gen.
Detector Link set

The detector link consist of 4 sections:

1. PEN ribbon from the detectors to the top of the mixing chamber;
2. Kapton boards at the mixing chamber that glue the PEN with section 3.
3. Twisted – tissue link between the mixing chamber and room temperature;
4. Cabling at room temperature from the fridge to the front-end inputs.

Detector

\[ K \text{=} \text{Kapton} \]

\[ \text{J} \text{=} \text{PEN} \]

\[ \text{J} \text{=} \text{Constantan like} \]
Detector Link state of the art

The state of the art is as follows:

1. PEN ribbon from the detectors to the top of the mixing chamber: designed and in production for CUORE0, final production pending for possible tuning after CUORE0 assembling;

2. Kapton boards at the mixing chamber that glue the PEN with section 3: designed and produced for CUORE0, final production pending for possible tuning after CUORE0 assembling;

3. Twisted – tissue link between the mixing chamber and room temperature: production completed, testing under way in Milano (why Milano?)

4. Cabling at room temperature from the fridge to the front-end inputs: design completed, material procured almost completely, assembling done for CUORE0, final production pending for possible tuning after CUORE0 and electronics position.
Detector Link room temperature section pictures

Detector

Standard commercial cable: ~150 pF/m

CUORE0 will compare the performances of the 2 solutions, hoping that the Carl-cable

Ribbon twisted cable (Carl-cable) from USC: ~50 pF/m (it requires additional shielding).

GS, 9 June 2011
So far all the considered links have been found good for us!
THE 4 K TO ROOM TEMPERATURE DETECTOR LINK CHARACTERIZATION SET-UP

We apologize but this report has been moved to the next meeting.
Very Front-end: Preamplifier (1)

Detector

Very front-end (on the fridge)

Pre

Bias and load resistors

SS

X6

Glue. Logic

Backplane

Main board

Preamplifiers production was completed at USC:

Total pre-amps produced (with and without JFETs): 1240

Pre-amps with JFETs: 1171
Without JFETs: 169

Pre-amps at UCLA: 1141
At USC: 30 with JFETs (these ship today), 169 without.
Passed parameters:

✓ Yield;
✓ Gain;
✓ Dynamic;
✓ Parallel noise;
✓ Series white noise.

Series 1/f noise was found larger than expected due to the contribution of a ADC exploited to tune the offset.

3 solutions has been studied and tested to solve the problem.

The cheaper, and more effective one, consists in the modification of the values of 6 resistors and 1 capacitor. This allows to swap, within the circuit, the role of the inquired DAC and a digital trimmer having much smaller noise.
PREAMPLIFIER CHARACTERIZATION AT UCLA

We apologies but this report has been moved to the next meeting.
Board reworking is very easy and requires low cost.

Table 2: Noise result of preamplifier with or without low pass RC filter

<table>
<thead>
<tr>
<th>Preamplifier number</th>
<th>Noise density at 1Hz (nV/√Hz)</th>
<th>Original setting</th>
<th>New setting 1</th>
<th>New setting 2</th>
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</thead>
<tbody>
<tr>
<td>1163</td>
<td>17.8</td>
<td>6.0</td>
<td>4.6</td>
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<tr>
<td>1187</td>
<td>18.4</td>
<td>7.3</td>
<td>5.1</td>
<td></td>
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<td>1428</td>
<td>20.1</td>
<td>6.4</td>
<td>5.5</td>
<td></td>
</tr>
<tr>
<td>1423</td>
<td>17.3</td>
<td>6.8</td>
<td>6.3</td>
<td></td>
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<tr>
<td>1378</td>
<td>21.1</td>
<td>6.2</td>
<td>4.9</td>
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<tr>
<td>1369</td>
<td>15.4</td>
<td>7.9</td>
<td>5.2</td>
<td></td>
</tr>
<tr>
<td>1952</td>
<td>20.4</td>
<td>5.5</td>
<td>4.9</td>
<td></td>
</tr>
<tr>
<td>1980</td>
<td>16.9</td>
<td>5.8</td>
<td>5.6</td>
<td></td>
</tr>
<tr>
<td>1352</td>
<td>15.8</td>
<td>6.5</td>
<td>5.3</td>
<td></td>
</tr>
<tr>
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<td>15.0</td>
<td>6.9</td>
<td>5.6</td>
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<td>16.5</td>
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<td>5.5</td>
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<td>1400</td>
<td>15.1</td>
<td>8.1</td>
<td>5.3</td>
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</tr>
</tbody>
</table>

Results are from XIAOLIU

The final result reflects the expected target.
Preamplifiers are going to be tested, characterized and trimmed at UCLA with temperature. UCLA got an environmental chamber just for this purpose.

Environment chamber: Model TEC1 from TestEquity Inc.
Multimeter: Model 2700 from Keithley Instrument Inc.
Signal generator: Model 395 from Wavetek Inc.
Power supply: Customized model from Gianluigi group.

Results are from XIAOLIU

GS, 9 June 2011
Preliminary results from gain drift characterization: results satisfy the expectations.

Gain: ~ 203.5 V/V at 30°C
Gain drift: < 10ppm/°C from 30°C to 40°C

Table 3 Gain of preamplifier (DC level test signal)

<table>
<thead>
<tr>
<th>Preamps</th>
<th>Gain (V/V)</th>
<th>20°C</th>
<th>30°C</th>
<th>40°C</th>
<th>50°C</th>
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<tbody>
<tr>
<td>1952</td>
<td>203.5482</td>
<td>203.5307</td>
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<tr>
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<td>203.4671</td>
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<td>203.6048</td>
<td>203.6012</td>
<td>203.6075</td>
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Table 4 Gain drift of preamplifier (DC level test signal)

<table>
<thead>
<tr>
<th>Preamps</th>
<th>Gain drift (ppm/°C)</th>
<th>20°C to 30°C</th>
<th>30°C to 40°C</th>
<th>40°C to 50°C</th>
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</thead>
<tbody>
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<td></td>
</tr>
<tr>
<td>1980</td>
<td>-9</td>
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<td>3</td>
<td></td>
</tr>
<tr>
<td>1352</td>
<td>-9</td>
<td>-4</td>
<td>1</td>
<td></td>
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<td>-5</td>
<td>-2</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>1435</td>
<td>-5</td>
<td>-1</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>1400</td>
<td>-10</td>
<td>-2</td>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>

Table 5 Gain of preamplifier (40Hz sine wave test signal)

<table>
<thead>
<tr>
<th>Preamps</th>
<th>Gain (V/V)</th>
<th>20°C</th>
<th>30°C</th>
<th>40°C</th>
<th>50°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1952</td>
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Table 6 Gain drift of preamplifier (40Hz sine wave test signal)

<table>
<thead>
<tr>
<th>Preamps</th>
<th>Gain drift (ppm/°C)</th>
<th>20°C to 30°C</th>
<th>30°C to 40°C</th>
<th>40°C to 50°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1952</td>
<td>-11</td>
<td>-7</td>
<td>5</td>
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<td>1980</td>
<td>-3</td>
<td>-9</td>
<td>11</td>
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<td>1352</td>
<td>-7</td>
<td>-6</td>
<td>4</td>
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<tr>
<td>1358</td>
<td>-10</td>
<td>-3</td>
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<tr>
<td>1400</td>
<td>-14</td>
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<td>8</td>
<td></td>
</tr>
</tbody>
</table>

Results are from XIAOLIU
Preliminary results DC drift characterization. This result has been obtained with a simple linear correction and satisfies the expectations although we would like to stay around or below 0.1 $\mu$V/°C, including second order effects in the correction proceeding.

Pre. output drift / Gain < 0.25uV/°C (from 30°C to 40°C)
We selected custom resistors from SRT, a Germany company.

At USC Ohmcraft was also selected whose custom resistors seems to show similar performances at lower price.
LOAD RESISTORS CHARACTERIZATION FOR CUORE

We apologies but this report has been moved to the next meeting.
Not coated resistors have shown a huge dependence on humidity.
Coated resistors have shown a negligible dependence on humidity.
Provided that the resistors are coated they seem to be adequate for CUORE.

We are starting their noise characterization vs bias for final qualification.
Electronic System Scheme

Detector

Very front-end (on the fridge)

Pre

SS

Bias and load resistors

X6

Backplane

Glue. Logic

Main board

Antialiasing

Calibration Pulse Gen.

Heater Pulser

Linear Supply, ±9 V, ±5 V

DC/DC 48 V to 12/6 V

48 V AC/DC

Power supply system

GS, 9 June 2011

= PEN

= Constantan

= Kapton

161x76 to 398x244
Very Front-end: Main board

Detector

The layout of the board is started.

Main board

Design completed.

GS, 9 June 2011
Electronic System Scheme

Links to the detectors: PEN and glue Kapton boards.

Detector

Pre

SS

Bias and load resistors

X6

Backplane

Glue. Logic

Main board

Antialiasing

x12

Glue Logic

Backplane

Small Faraday Cages

Close to the DAQ

DAQ

Bessel Filter

Linear Supply, ±9 V, ±5 V

DC/DC 48 V to 12/6 V

48 V AC/DC

Power supply system

Heater

Pulser

Calibration Pulse Gen.

K = Kapton

Kapton

J = PEN

Constantan

GS, 9 June 2011
We apologize but this report has been moved to the next meeting.
2 prototype are in Milan from USC for testing of functionality:

They have been characterized and tested against: firmware, gain, frequency response and noise.
Frequency response uniformity on the 4 selectable bandwidths: compliant on the 24 channels.

GS, 9 June 2011
Noise has been measured on a few channels, till now, but it was fine.
Bessel filter boards can be completed for CUORE0 run.

Production for CUORE is postponed after CUORE0 results for bandwidth tuning.

All the components not involved on the bandwidth tuning have been procured at USC.
Electronic DC/DC results upgrade (1)

Detector

Very front-end (on the fridge)

Bias and load resistors

Backplane

Glue. Logic

Main board

V X6

Pre SS

Antialiasing

Bessel Filter

x12

Glue Logic

Backplane

Small Faraday Cages

Close to the DAQ

Linear Supply, ±9 V, ±5 V

Calibration Pulse Gen.

Heater Pulser

Power supply system

48 V AC/DC

48 V to 12/6 V

DC/DC

GS, 9 June 2011
This is the slide we showed the last August. As it can be appreciated the pp noise at the output of the DC/DC was around 50 mVpp.
Optimization has been done and now the pp noise is less than 2 mVpp, about 25 times smaller level.

4.3 A load 350 MHz BW

+12 V

-12 V
In 20 MHz BW the noise is smaller than 1 mVpp!
Electronic DC/DC results upgrade (5)

Limiting the load to 2.6 A results are much better:

2.6 A load 350 MHz BW

+12 V

-12 V
Electronic DC/DC results upgrade (6)

In a 20 MHz BW at 2.6 A load the noise is 0.65 mVpp!

2.6 A load 20 MHz BW

+12 V

-12 V

GS, 9 June 2011
Items list and status (1)

1. PEN very low background link at 10 mK (for CAW): design and test system completed, final production pending for tuning after CUORE0;
2. Detector Link from the fridge to the preamplifier inputs: cables and connectors selected and procured at USC, already available for CUORE0;
3. Front-end Backplane, pending;
4. Main board for preamplifier: layout stage starting;
5. Preamplifiers: design and production done, characterization in progress;
6. Detector biasing: design done and resistors under final selection based on economical parameters;
7. Load resistors: under final selection;
8. Cabling from front-end to Bessel filters, pending;
9. Backplane for Bessel filter: done;
10. Bessel filter: prototypes available and tested, production for CUORE0 is going to start;
11. Faraday cage for Bessel filter, on the way to Gran Sasso;
12. Cabling from Bessel filter to DAQ, pending;
13. Pre regulation of the power supply: prototype under construction at USC;
14. Linear Power Supply, pending;
15. Calibrating Pulse generator: final design phase;