Cryogenic ASICs in GaAs for Applications with Particle Detectors

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Abstract: We present two cryogenic Application Specific Integrated Circuits (ASICs) realised with a GaAs MESFET process. A single-channel differential or double-channel single-ended voltage sensitive preamplifier for a 3 K operation, to be used with bolometric detectors, was realised and tested. A very simple structure working in a unity gain buffer or as a transconductance amplifier, or even as a slewing filter was tested in view of an application with a fast particle detector operated at liquid He temperature.

1. INTRODUCTION

There are several experiments in elementary particle physics which use detectors operating at cryogenic temperatures. For optimum operation, these instruments need to be readout with amplifiers able to operate in the same environment, at low temperature. Bolometers are very high energy resolution detectors [1] which operate at temperatures as low as 10 mK. The energy deposited in the detector by an impinging particle suddenly increases the crystal temperature. The change of temperature is converted into an electrical signal by a resistive sensor put in good thermal contact with the detector absorber. The relaxation to the initial conditions is made through a thermal link which connects the system to the heat sink.

There are a few classes of such detector, depending on their composition and dimensions. Large mass bolometric detectors consist of two main parts: the absorbing crystal and the temperature sensor. Monolithic bolometers are realised with crystals, often silicon, of very small mass and the temperature sensor is directly implanted in a small region. Various type of thermal sensors can be used to read the temperature change: Silicon or Germanium Thermistors, Superconducting Tunnel Junctions (STJ) or Transition Edge (TE) superconducting films.

Thermal detectors are slow, rise time being limited by the speed of sound in the absorbing crystal. The frequency bandwidth of the signals generated is limited to a few kHz. The intrinsic energy resolution achievable can be very high, of the order of a few electron-volts. The impedance have a dominant resistive component ranging from a few Q (TE sensor) to hundreds of MΩ (Thermistors).

Frequently, a limit in achieving the intrinsic energy resolution arise from noise in the detector correlated to external disturbances. For instance, mechanical vibrations in the detector occurs, by friction, spurious noise spikes and, in the case of thermistor sensors of large impedance, the vibration of the electrical link generates microphonic noise in the electrical parasitic capacitance shunting the sensor.

In this paper two monolithic amplifiers designed for applications with two different detectors and experimental conditions are presented. They have been realized using a GaAs MESFET process.

In Section 3 a Buffer/Led Driver (B/LD) circuit for fast signal handling is presented.
2. The Differential-Single-Ended Voltage Sensitive Preamplifier (DSSVP)

2.1 Description of the circuit configuration.

For the above mentioned reasons the preamplifier circuit must have low series noise in the low frequency region and must be capable to operate at temperatures as close as possible to 1 Kelvin, to minimize the length of the link. Moreover, the microphonics originating in the electrical link can be strongly attenuated by adopting a preamplifier with differential input. This way a pair of wires firmly tied together, connecting the sensor to the preamplifier, generates only common mode disturbances. When the wires vibrate, those disturbances will cancel out at the preamplifier output. Nevertheless, with low resistive sensors the differential configuration may not be requested and a single-ended configuration would be preferred.

Having in mind the above requirements we have designed and realized a DSSVP capable to operate as a differential voltage preamplifier or as a two channel single-ended voltage preamplifier.

Figure 1 shows the schematic of the DSSVP. When operated as a single-ended preamplifier, two identical channels are available. The network of Figure 1 is symmetrical at the left and right of the two output pads OUT and OUT'. For this operating mode pad S1 must be connected to Vss, while pad S2 to

diode D1. Each channel features a closed loop gain of 11 which is given by \( \frac{R_c}{R_e} = \beta \), \( R_c = 100 \Omega \). High open-loop gain is assured by the dual stage configuration. Q1 is the input transistor, Q2 boosts it and Q3 cascades the structure. R1, R2 and Q1 form a bootstrapped current source which loads this input stage. The inverting stage is a common source amplifier, Q3, loaded with another bootstrapped current source R5, Q4 and Q5. Transistor Q5 buffers the output of the whole preamplifier. The two diodes at the drain of Q2 and the current generator Ibl serve as level voltage transistors. The input transistor Q2 has an area (LxW) 3.6 x 0.005 mm² to assure low series noise. A L=3 μm gate-length was selected as the most suitable for low 1/f noise [1, 2]. The whole monolithic chip area is 2.5 x 2.5 mm². The resistor R1 is used to inject a suitable biasing current, in the range 1.9 mA to 7.5 mA, into Q1. The preamplifier was designed to get minimum power dissipation. The positive supply voltage Vcc may be 4 V or 1 V, depending on the noise and dynamic requirements. Vss for the single ended configuration is approximately 0.3 to 0.6 V.
adjustable to get proper DC output voltage, at half of the allowed output swing, which ranges from 1.4 to 2V (VCD~3.5V) or 3V (VCD~4.5V). Power dissipation is 31 mW and 32 mW for VCD equal to 4 V and 5 V respectively.

For differential operation pad S1 has to be left open, pad S2 must be connected to ground. In this way the resistor R helps sink the network current and the two stages become coupled at the sources of the two input transistors Q1. The positive supply voltage VCC can range now from 3 to 4 V, while the negative supply voltage VEE varies between -2.5 to -3V, depending on the undesired output voltage operation. Power dissipation ranges from 21 mW to 17 mW. The output differential voltage (OUT- - OUT+) is now 11 times the input differential voltage (IN+ - IN-). The signal swing is the same as for the single ended configuration, but the output DC bias now stabilize between 0.6 V to 1 V (VCD=3 V) or 2 V (VCD=4 V), equivalent to the voltage across the missing diode.

The most relevant characteristic obtained with this design is that the very high input impedance differential preamplifier is similar to an instrumentation amplifier, but use only one long-tailed pair is the input, saving a factor of 2 in the series noise.

For both configurations two additional pads are available, OA and OB, which allow to equalize the output voltage at the same DC level. Alternatively, either one or both of them can be used to trim the output while maintaining fixed the negative supply VEE at a desired value.

As can be observed by inspection the preamplifier is totally DC coupled. 2.2 Results obtained

Concerning the dynamic behavior, the D/SVSP showed very good results. The 1/f noise, instead, was not as low as expected according to noise performance of previous monolithic units. For the differential configuration when VEE=3V the integral non-linearity was less than 0.5% referred to a 300 mV range, as can be seen in Figure 2 where the response to a 100 kHz sinewave signal is shown. The common mode rejection ratio (CMRR) was also high, being about 35 dB from DC to a frequency of a few kHz, remaining larger than 65 dB up to 100 kHz, Figure 3. For the single-ended configuration the same results applies except that CMRR should not be considered. The level of possible cross-talk between the two channels was very small, difficult to quantify by direct measurements.

![Figure 2: Response to a linear fit relative to a 300mV output voltage range for the differential configuration.](image)

![Figure 3: Differential Common Mode Rejection ratio.](image)
3. THE BUFFER/LED DRIVER (B/L/D)

The B/L/D was designed following the requirements of a Liquid Argon Proxhower detector under development at CERN [4]. The temperature of operation of the whole system is 77 K, the LAr temperature. The aim of the circuit is to convert the voltage signal at the output of the preamplifier into a current, suitable to drive a LED. This is located in LAr, and it is used to drive a fiber optic, converting the signal current into an optical signal. The requirements to the B/L/D are to be fast, to the expected rate of the incoming events will be high, to dissipate very low DC standing power because a large number of channels are foreseen, and to be able to drive a large signal current, up to 100 mA with an integral non-linearity of less than 1%.

The monolithic circuit we have realized satisfies all those requirements. Its schematic diagram is shown in Figure 6. The photograph of an output buffered voltage signal of 2 V is illustrated in Figure 7. As can be seen in Figure 6 only a few transistors were used to implement the network. The circuit is a non-symmetrical differential amplifier having the non-inverting input at the source of Q2, while the inverting input is at the gate of Q1. Q1 is loaded by a bootstrapped current source R1, R2, and Q1, Q2 is the output buffer transistor. In the configuration shown the network has a unity feedback return ratio (between the
gate of the input transistor Q1 and the output, at the source of the transistor Q2, via the two shunting diodes D1 and D2. The circuit can operate as a unity gain buffer, taking the output voltage at V1 or as a transconductance amplifier having a gain \( g_{m} = \beta R_{C} \) by reading the output current at the drain of Q2.

We can calculate the closed-loop gain. The open-loop gains for the non-inverting input A' and for the inverting input A are:

\[
A' = \frac{V_{V1} - \frac{R_{C} R_{1}}{1 + g_{m} R_{C}}}{V_{1}} = \frac{g_{m} R_{C} R_{1}}{1 + g_{m} R_{C}} \quad \text{and} \quad A = \frac{V_{V1} - \frac{R_{C} R_{1}}{1 + g_{m} R_{C}}}{V_{Q2}} = \frac{g_{m} R_{C} R_{1}}{1 + g_{m} R_{C}} \quad \text{for} \quad \beta R_{C}
\]

in eq (1) \( R_{D} \) is the dynamic Drain to Source resistance of Q1. The Dynamic impedance \( R_{DS} \) of the bootstrapped current source \( R_{D}, Q_{2}, \) and \( Q_{2} \) was neglected as much greater than \( R_{DS} \). The gain \( A' \) is about 25 when the output loading impedance \( R_{C} \) is 100 \( \Omega \) 11 when it is 20 \( \Omega \). Finally, the closed-loop gain from \( V_{V1} \) to \( V_{4} \) becomes, taking into account that the feedback return ratio, \( \beta \), is unity:

\[
A_{CL} = \frac{A'}{1 + \beta A'} = \frac{1}{1 + \frac{1}{g_{m} R_{C}(1 + g_{m} R_{C})}}
\]

(2)

\( A_{CL} \) results larger than 0.9 when the load resistor \( R_{C} \) is as low as 20 \( \Omega \). This is obtained by considering that the term \( \mu g_{m} R_{DS} \) is about 28 and \( g_{m} \), 35mK\( \Omega \) in eq (2). The feedback action increases the open loop input impedance \( (1 + \frac{R_{DD}}{R_{DS}}) \) and decrease the output impedance 1\( g_{m} \) to:

\[
R_{i} = \frac{R_{DD} + R_{DS}}{1 + g_{m} R_{C}} \quad \text{and} \quad R_{o} = \frac{1}{g_{m} R_{C}(1 + g_{m} R_{C})}
\]

(3)

\( R_{f} \) is estimated slightly less than 500 k\( \Omega \), much greater than the impedance of the source, 50 \( \Omega \). The simulated output impedance \( R_{o} \) was about 6 \( \Omega \), the measured one was 4 \( \Omega \), included stray effects.

The occupation area of the chip is 1x0.4 mm\(^2\), with an input transistor having an area of 2x1000 \( \mu m \). All the characteristics were measured at a temperature of operation of 77 K. The positive supply voltage was set to 5.5 V, the negative one to -2.5 V. The total power dissipation was 12.6 mW.

The B/LD was configured for different operations. Figure 7 shows that the circuit is able to work as a unity gain buffer, even with large signals. Very good results were obtained when the network was operated as a transconductance amplifier. Figure 8 shows the integral non-linearity of the output signal current. The current was developed across a 2.50 resistor connected between the drain of Q2 and the positive supply voltage VCC. The signal was filtered by a RC-CR shaper (one integrator and one differentiator) having 20 ns peaking time. As can be seen the error of less than 1% referred to a range of 100 mV. The rise time even for the large signal was less than 9 ns, as illustrated in Figure 9.

With B/LD was also possible to realize a RC-CR shaping filter of 50 ns peaking time. The implementation was realized as follows. Resistor R, and capacitor C were set 20 \( \Omega \) and 2 \( \mu F \) respectively, acting as differentiator. A 50 \( \Omega \) resistor was connected between the drain and the supply voltage of Q2. The receiving end of a coaxial cable was AC coupled to the Q2 drain with an integrator formed with 50 \( \Omega \) shunted with 2 \( \mu F \). This way the line realted terminated and the low-pass filter was effective in filtering the electromagnetic interferences acting on the cable. No distortions or reflections were observed in the output pulse also for 10 m of cable length.

The series noise, measured at a 50 MHz frequency range, had a 1/4 component with \( A_{n} = 10^{-8} \sqrt{V} \) and a white component of slightly less than 1.5 \( mV/\sqrt{Hz} \), resulting in about 4.5 MHz corner frequency.
4. CONCLUSIONS

Two new linear ASIC's for cryogenic use have been realized using GaAs technology. A voltage preamplifier able to work as a two channel single-ended input preamplifier or as a differential preamplifier was able to work down to 4.2 K. Power dissipation can range between 20 mW and 37 mW, depending on dynamic and noise requirements. At 4.2 K in the 100 kHz frequency range the noise was 10^14 V/√Hz. A fast unity-gain voltage buffer and transconductance amplifier was realized to operate at 87 K. It is able to amplify large signals and to drive a 100 mA current into a LED, for and optical signal transmission from a cryogenic environment. Power dissipation is 12.6 mW, the rise time of a signal of 100 mA, on 2.5 Ω, is 8 ns. The output series noise has a 1/f component, having an intensity A_f of about 10^17 V^2, followed by a white noise term slightly less than 1.5 mV/√Hz. The corner frequency is about 4.5 MHz.

The voltage-sensitive preamplifier was designed to read-out the signal of bolometric detectors, while the Buffer/Led Driver was intended to amplify signals coming from a Liquid Argon Flasher detector at CERN.

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6. REFERENCES


