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Considerations on the front-end readout for cryogenic particle detectors

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It exists different types of cryogenic particle detectors. Each class of detector generates signals having different shape, in response to the impinging energetic particles. Their dynamic impedances vary greatly, too. For this reason it is not possible to speak about a standard front-end approach to the readout for a cryogenic detector. The preamplifier configuration, the choice of the input transistor of the preamplifier and the front-end location, at cold close to the detector or at room temperature, must be decided for each particular situation. The tentative of this contribution will be to give some general rules for the suitable choice of the front-end that better fits any cryogenic application, once the characteristics of the detector, speed of signals and impedance, are known.

One common aspect of any selected preamplifier configuration chosen to readout a detector class is the Signal to noise Ratio, S/N. Let's model the detector as a current source, \( i_0 = E_p S(\omega) \), \( E_p \) being the particle energy, \( S(\omega) \) the detector transfer function in the frequency domain. Let's define also \( Z_0(\omega) = Z_0/\omega \), \( Z_{par}(\omega) \) the parallel combination of the detector impedance, \( Z_0(\omega) \), the parasitic capacitance of the link that connects the detector to the front-end, \( C_p \), and the open loop input capacitance of the preamplifier, \( C_A \). For any possible filter connected at the output of the acquisition chain, by applying the Schwartz inequality, it is easy to show that the square of the S/N is always limited by [1]:

\[
\left( \frac{S}{N} \right)^2 \leq 4 \int_0^\infty \frac{E_p^2 (\omega)^2}{Z_0(\omega)^2} \left[ \frac{1}{Z_{par}(\omega)} \right] \left[ 1 + \frac{1}{Z_A(\omega)} \right] df
\]

(1)

In eq. (1) \( E_p(\omega) \) and \( Z_A(\omega) \) are the series and parallel noise of the front-end preamplifier, and \( Z_{par}(\omega) \) is the detector parallel noise. All the noise sources are considered monolateral. The equal sign applies when the so-called optimum filter is connected at the preamplifier output. As an
example, the result obtained in eq.(1) is valid for both the classical charge/current sensitive preamplifier and the voltage sensitive preamplifier.

From eq.(1) a number of considerations can be made. The first important one is that the S/N does not depend on $Z_d(\omega)$ if the series noise is negligible. The second one concerns the optimization of the area of the preamplifier input transistor. The larger the area of the transistor, the smaller is the value of the series noise and the larger is its input capacitance, $C_A$, that in general coincides with the input impedance of the open loop preamplifier. The smaller is the area, the larger is the noise:

$$\frac{\sigma_A^2(\omega)}{\sigma_0^2(\omega)} = \frac{C_A}{C_0}. \tag{2}$$

From above it is evident that there is an optimum choice for the area of the input transistor. If the input transistor has a too large area, the denominator in eq.(1) becomes large, limited by $C_A$. If the input transistor has a too small area the denominator in eq.(1) is again large, limited by the amount of series noise present. A similar argument can be made for the parallel noise of the preamplifier. For this case it must be considered that the parallel noise dependence on $C_A$ is the opposite with respect to the series noise:

$$\frac{\sigma_A^2(\omega)}{\sigma_0^2(\omega)} = \frac{C_A}{C_0}. \tag{3}$$

The last important consideration regards the location of the preamplifier. The parasitic capacitance of the connecting link, $C_P$, has its value that is proportional to the link length and might dominate the input impedance at the very extreme, $Z_d(\omega)=1/j\omega C_P$. In this case the series input noise has its contribution enhanced by this effect:

$$\left(\frac{S}{N}\right)^2 \leq 4 \int_0^\infty \frac{S(\omega)^2}{\sigma_A^2(\omega) + \sigma_0^2(\omega)} \, df \tag{4}$$

By the above arguments it is clear that the location of the preamplifier close to the detector, in the cryogenic environment, is, by far, the better choice [2], [3]. Nevertheless the best noise performances of the selected transistors often are not obtained at too low temperature. Moreover, the use of a room temperature front-end is of much practical implementation [4], [5], especially for the case an array of detectors is used [6], and, in many cases, does not result in a worst performance.

Care must be put in maintaining low the microphonic noise. If the preamplifier has a single ended input the possible vibration of the connecting link varies the parasitic capacitance $C_P$. For a typical sinusoidal fluctuation of frequency $\omega_0$, supposed for simplicity constant in amplitude, a
noise signal is added at the preamplifier input of an amount proportional to the capacitance fractional change:

\[
\Delta V_i = \frac{\omega_i R_D C_P}{\sqrt{1 + (\omega_i R_D C_P)^2}} V_{\text{BIAS}} \frac{\delta C_P}{C_P} \sin(\omega_i t)
\]  

(5)

In the above eq. a resistor, \( R_D \), approximates the detector impedance, and \( V_{\text{BIAS}} \) is the detector applied bias. The microphonic effect can be greatly attenuated if the differential readout is used. For this case a pair of twisted wires are used to connect the detector to a differential preamplifier. The two wires vibrate the same way and produce the same microphonic noise signal that cancel out at the preamplifier inputs. The differential voltage sensitive configuration is useful also because it allows suppressing the cross-talk effect when the connecting links of many different channels are closed together.

The last important aspect concerns the technology of the transistors. Many different solutions are available for both the cold and room temperature front-end readout. An indication of the main characteristics available will be given below.

When concerning cryogenic operation possible choices are between: Si MOS, Si JFET, Ge JFET, GaAs MESFET, GaAs HFET, SiGe HBT and GaAs HBT. At cryogenic temperatures the freeze-out may limit the number of free carriers available for conduction following [7]:

\[
n = \frac{N_d N_c}{g_D} e^{-\frac{E_D}{k_B T}}
\]  

(6)

In eq.(6) \( n \) is the concentration of free electrons present in the conduction band, \( N_d \) is the donor concentration, \( N_c \) the effective density of state in the conduction band, \( E_D \) is the energy difference between the conduction band and the donor energy, \( k_B \) is the Bolzmann constant, \( T \) the absolute temperature and \( g_D \) is the degenerate factor at the donor energy level (i.e. \( g_D \approx 2 \) for Si and 4 for GaAs). Each semiconductor has a different value of \( E_D \). As a consequence the lower temperature of operation can differ in a significant way. Table 1. It has to be remarked that the electric field applied to the transistor for biasing helps to free charges from the donor sites. As an example is the Si MOS that is able to work down to 4.2 K although the quite complete freeze-out which happens in silicon [8].
Table 1: Attenuating coefficient for the concentration ς for different temperatures.

<table>
<thead>
<tr>
<th>SEMIC</th>
<th>$E_d$ (meV)</th>
<th>$e^{-E_d/(2kT)}$ @ 76 K</th>
<th>$e^{-E_d/(2kBT)}$ @ 10 K</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs</td>
<td>6</td>
<td>0.6</td>
<td>$10^{-2}$</td>
</tr>
<tr>
<td>Ge</td>
<td>9</td>
<td>0.5</td>
<td>$10^{-1}$</td>
</tr>
<tr>
<td>Si</td>
<td>45</td>
<td>$10^{-1}$</td>
<td>$10^{-11}$</td>
</tr>
</tbody>
</table>

Each device has its own proper optimum temperature of operation, larger than the freeze-out temperature. All the indicated devices shows low frequency noise, LF, at low temperature. This source of noise in general increases in magnitude below the optimum operating temperature due to scattering with donor impurities [9]. while for some devices having large LF at room temperature it improves at low temperature, but still it remains large. A compromise must be made between LF noise performance and temperature of operation for any device selected. A parameter of comparison for LF noise is $H_T = A_T C_T$ [9]. $A_T$ being the low frequency noise coefficient. $H_T$ is a normalizing parameter which coincides with the noise of the device measured at 1 Hz when the transistor area is ideally chosen to obtain $C_T = 1$. For MOS transistor and GaAs MESFET or HEMT devices $H_T$ is found between $10^{27}$ to $10^{26} J$, while for Si JFET it is generally close to $10^{27} * j10^{28} J$, although values close to $10^{29} J$ has been measured at cold [10]. No data are known to the author with regard the LF behavior at cold for SiGe HBT.

For fast detectors white noise is of more concern and again transistor’s thermal noise has a minimum at a proper temperature. For fast signals GaAs devices can give good results down to liquid helium since their superior transconductance value allows to obtain low the thermal noise [11].

A room temperature front-end solution can be implemented using the same variety of transistors. In this case a low LF performance is often obtained using Si JFET. For the requirement of low white noise, and for the case of small detector impedance (for instance with the SQUID as a sensor), an additional choice can be the use of the more classical Si bipolar transistors, which can offer low LF noise and small white noise at the same time, at the expense of large parallel noise [4].

REFERENCES


