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A low noise and high precision linear power supply with thermal foldback protection

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A low noise and high precision linear power supply was designed for use in rare event search experiments with macrobolometers. The circuit accepts at the input a “noisy” dual supply voltage up to $\pm 15$ V and gives at the output precise, low noise, and stable voltages that can be set between $\pm 3.75$ V and $\pm 12.5$ V in eight 1.25 V steps. Particular care in circuit design, component selection, and proper filtering results in a noise spectral density of 50 nV/\(\sqrt{\text{Hz}}\) at 1 Hz and 20 nV/\(\sqrt{\text{Hz}}\) white when the output is set to $\pm 5$ V. This corresponds to 125 nV RMS (0.8 $\mu$V peak to peak) between 0.1 Hz and 10 Hz, and 240 nV RMS (1.6 $\mu$V peak to peak) between 0.1 Hz and 100 Hz. The power supply rejection ratio (PSRR) of the circuit is 100 dB at low frequency, and larger than 40 dB up to high frequency, thanks to a proper compensation design. Calibration allows to reach a precision in the absolute value of the output voltage of $\pm 70$ ppm, or $\pm 350$ $\mu$V at $\pm 5$ V, and to reduce thermal drifts below $\pm 1$ ppm/°C in the expected operating range. The maximum peak output current is about 6 A from each output. An original foldback protection scheme was developed that dynamically limits the maximum output current to keep the temperature of the output transistors within their safe operating range. An add-on card based on an ARM Cortex-M3 microcontroller is devoted to the monitoring and control of all circuit functionalities and provides remote communication via CAN bus. Published by AIP Publishing. [http://dx.doi.org/10.1063/1.4948390]

I. INTRODUCTION

Particle physics experiments searching for unknown, rare phenomena, such as dark matter or neutrinoless double beta decay, usually require front-end electronics with exceptionally low noise. And since they often need to take data for several years to accumulate statistics, also very good stability versus time and temperature is required. This ensures that the data taken over long runs are consistent, and that any observed drift can be ascribed to physical phenomena or to the operating behaviour of the detectors, without additional contributions coming from the electronics. Such requirements apply not only to the front-end amplifiers, but also to the detector biasing circuits. A good control of the quality and precision of the power supplies and reference voltages from which the front-end circuitry operates is mandatory to this purpose.

The circuit presented in this paper is a linear power supply, designed for use with large mass thermal detectors (bolometers) in the CUORE, LUCIFER, and CUPID experiments. The entire power supply chain for the above experiments was described elsewhere, The instrument presented here is the last stage of the above power supply systems. The circuit supplies precise, stable, and low noise voltages to operate the front-end electronics. The frequency range of interest with such detectors extends from DC up to a few kHz. Particular care was therefore given to the minimization of low frequency noise contributions and of all sources of drift or instability. The circuit is the improved version of a similar instrument successfully used with bolometers in the past. Aside from several improvements to the analog circuitry, the device is now also equipped with digital functionalities that allow it to be remotely monitored and controlled, minimizing the need for human interventions that would perturb the experiment. Some of the features of the present circuit were already anticipated elsewhere, but a deeper description is given in this paper, together with characterization results.

II. CIRCUIT DESCRIPTION

Figure 1 shows a block schematic of the circuit, with emphasis on the input side. A set of protections are implemented at the input to prevent incorrect voltages from damaging the circuit. A diode bridge is used to generate the RECT voltages that allow the digital board to operate even if the polarity of the input voltages is incorrect. The RECT voltages are also used to power a decision network composed of a set of LM339 comparators from Texas Instruments. If the IN voltages are of the correct polarity, correct range (+5 V to ±17.5 V), and are symmetrical with respect to ground within a 10% error, then the relays $S_R$ and $S_N$ are closed, and the analog block is powered. $S_R$ and $S_N$ are each implemented as a pair of relays with coils having different operating voltages, selected by additional comparators in the decision block to cover the entire input voltage range.

A simplified schematic of the analog part of the circuit is shown in Figure 2. The VREF block generates a precise $\pm 2.5$ V voltage reference. The positive $2.5$ V reference is generated by a set of four LTC6655 voltage regulators from Linear,
connected in parallel to take their average output voltage and to reduce their noise by a factor of two, as advised in the component datasheet. The positive reference is buffered by a ADA4084 operational amplifier from Analog Devices, $A_1$. The negative 2.5 V reference is obtained by inverting the positive reference with $A_2$, again a ADA4084, used as an amplifier with gain of $-1$. The choice of the ADA4084, together with high precision 1 kΩ metal foil resistors $R_{V1}$ and $R_{V2}$ (Vishay SMR1DZ series), ensures that the noise and thermal drift of the resulting $\pm 2.5$ V reference voltages are low and dominated by the LTC6655 regulators. Noise is about 90 nV/√Hz at 0.1 Hz, 35 nV/√Hz at 1 Hz, 20 nV/√Hz white, and drift is below 2 ppm/°C, with a minimum close to 25 °C. Since they come from the same source, the noise and drift of the $\pm 2.5$ V reference voltages are almost fully anticorrelated. This will be used in the following to identify the origins of the noise contributions at the outputs.

The FILTER blocks are low pass filters used to eliminate the noise of the $\pm 2.5$ V references above their cutoff frequency, as well as the possible noise increase of the rail-to-rail output buffer at high frequency.\footnote{A trade-off is involved here. Filtering with a passive RC down to very low frequency (below 1 Hz) requires large value resistors and capacitors. But large electrolytic capacitors usually have a non-negligible leakage current, which would cause an unacceptable voltage drop on the resistor, affecting precision and drift. Also large value ceramics can show leakage, although typically lower than electrolytics. To work around this trade-off, different solutions have been considered for the FILTER block, which will be presented in the following.}

Taking at the input the filtered $\pm 2.5$ V reference voltages, the two DRIVER blocks regulate the voltage at their outputs through the power transistors $M_P$ and $M_N$. The 0.1 Ω resistors $R_P$ and $R_N$ at the source of the power MOSFETs are used to sense the output current. The output voltage can be set in the range $\pm 3.75$ V to $\pm 12.5$ V by selecting the value of the feedback resistors $R_{G1}$ from 500 Ω to 4 kΩ in eight 500 Ω steps, while the value of $R_{G2}$ is fixed at 1 kΩ. To minimize parasitic effects, the resistor values are switched with three bistable dual relays, not shown. The resistors used for $R_{G1}$ and $R_{G2}$ are high precision SMR1DZ metal foil resistors from Vishay, with absolute precision of $\pm 100$ ppm and thermal drift of $\pm 0.2$ ppm/°C.

At low frequency, below the cutoff of the FILTER blocks, the noise of the output voltages is expected to come from the $\pm 2.5$ V references. Above the cutoff, it is expected to come mainly from the operational amplifiers $A_3$ and $A_4$ used in the DRIVER blocks. Again, different options were considered: the ADA4084 from Analog Devices and the OPA2188 and OPA2140 from Texas Instruments. All these choices show input offset drifts below $\pm 1 \mu$V/°C. Compared to their input voltage of 2.5 V, this corresponds to less than 0.4 ppm/°C. This contribution is then negligible compared to the drift of the voltage references. All the operational amplifiers tested here also have rail-to-rail outputs. This is required to be able to fully switch off the power transistors if no current is drawn.

The feedback loop at the drain of $M_P$ and $M_N$ can be closed directly on the load with a Kelvin connection, in order to avoid the voltage drop due to the series resistance of the output wires at high currents. For this purpose each side of the circuit has two outputs, OUT and SENSE, to be connected together at the load side. To achieve high precision, the series resistance of the SENSE path must be considered, since it is in series with $R_{G1}$ and thus affects the gain of the DRIVER block. The resistivity of copper has a thermal coefficient of about $+4000$ ppm/°C. To ensure that its effect does not contribute to the overall drift, the total resistance between $R_{G1}$ and the load on the SENSE path must be kept below 10 mΩ.

Also the ground reference is connected to the load with two wires, GND SENSE and GND OUT. The latter is used to carry the load current and is connected to the ground plane of the board and to the input ground. GND SENSE is the precise reference of the VREF, FILTER, and DRIVER blocks.
The two grounds are connected together at the load. To avoid offset at the output, the series resistance of the GND SENSE wire must be low enough to conduct the supply current of the VREF block (about 20 mA for four LTC6655 regulators) without a significant voltage drop between the VREF block and the load. A 10 Ω resistor was connected between GND SENSE and GND OUT on the board, to limit the voltage drop to 200 mV in case the GND SENSE connection is accidentally disconnected. To prevent instability of the LTC6655 regulators above 1 kHz due to the series resistance and inductance of the GND SENSE path, a ceramic 100 µF capacitor was connected between the two grounds, close to the LTC6655 regulators.

If the \( V_p \) or \( V_N \) SENSE connections to the load are accidentally disconnected and left floating, the OUT voltages could saturate to the IN voltages, possibly damaging the circuits that are powered by the OUT lines. To prevent this risk, a simple circuit was added at the SENSE connector, shown in Figure 3 and based on a dual monostable relay. If either one of the SENSE lines is disconnected from the load, no current flows in the coil of the relay, and the SENSE connections are locally shorted to the OUT voltages. If the SENSE lines are connected at the load side, then the relay is powered: the SENSE outputs are connected to the SENSE lines, closing the Kelvin connection at the load and enabling remote sensing.

![Schematic of the circuit that automatically enables or disables remote sensing.](image)

**FIG. 3.** Schematic of the circuit that automatically enables or disables remote sensing.

Figure 4 shows a photograph of the circuit, laid out on a four layer 100 × 220 mm\(^2\) Eurocard standard printed circuit board (PCB). The power transistors \( M_P \) and \( M_N \), respectively, a 18 A/55 V AUIRFR5505 P-channel MOSFET and a 17 A/55 V AUIRFR024N N-channel MOSFET, both from International Rectifier and packaged in DPAK (TO-252), are mounted on a separate single-layer PCB on aluminium substrate, together with two BC858 diodes in SOT-23 package that are used to measure their temperature. The aluminium card is connected with wires to the main circuit and is mounted directly on the front panel, where also the heat sink is located. The use of a large heat sink allows to avoid the need for active cooling that might affect the noise performance at low frequency.

Figure 5 shows the thermal images of the circuit under different working conditions, acquired with a Fluke VT04 IR thermometer. No forced air flow was present. The outputs were set at ±5 V, and all the images were taken after 30 minutes in thermal equilibrium. In the top row, a 5 Ω load was connected between the outputs, to operate the circuit with a current of 2 A. On the left side, the input voltage was ±6.5 V, resulting in a power dissipation of 3 W on each MOSFET, 6 W in total. The temperature of the aluminium PCB was 45 °C and the heat sink was at 40 °C. On the right side, the input voltage was increased to ±8.5 V, resulting in a power dissipation of 14 W. The temperature of the aluminium PCB was now 68 °C, and the heat sink was at 53 °C. In the bottom row, a 2.5 Ω load was connected between the outputs, to operate the circuit with a current of 4 A. On the left side, the input voltage was again ±6.5 V, for a power dissipation on the aluminium PCB of 12 W. The temperature of the aluminium PCB was 60 °C, and the heat sink was at 43 °C. The hottest points of the circuit were now the sense resistors \( R_P \) and \( R_N \), each dissipating 1.6 W. The capability of the main PCB to dissipate their heat was overestimated: an exposed copper pad should have been included in the layout, for a better dissipation. On the right side, the input voltage was increased to ±8.5 V, leading to a power dissipation of 28 W. The hottest point of the circuit is now again the aluminium PCB that reaches 98 °C, while the heat sink reaches 70 °C. From the comparison between the two measurements at 2 A, we can estimate a thermal resistance between the heat sink and ambient of about 1.6 °C/W, and a total thermal resistance between the MOSFETs and ambient of 2.8 °C/W. This is compatible with what is expected from a heat sink of this size without a forced air flow.

Although in all of the above measurements the circuit was functional, it should be noted that the expected operating conditions correspond to those shown in the top left corner, where all the components were below 50 °C. This allows to
reduce the stress on the circuit elements and the related probability of failures.

On the other end of the board of Figure 4 is a small add-on card based on a LPC1768 ARM Cortex-M3 microcontroller from NXP semiconductors that provides all the digital functionalities of the circuit. The digital board can communicate with a remote control system (a PC, for instance) via CAN bus. It controls the three relays that allow to select the output voltage between ±3.75 V and ±12.5 V in eight ±1.25 V steps, as already mentioned. Through a multiplexer it can monitor all the significant voltages of the circuit with an AD7732 24-bit ADC from Analog Devices, providing precise diagnostics and current sensing. The ADC can use either a 2.5 V reference located on the digital board, with temperature drift of about 10 ppm/°C, or the more precise 2.5 V reference generated by the VREF block on the main board. Thanks to proper filtering, the measurement of sensitive nodes of the analog section was found to have a minimal or no impact on the output noise. The microcontroller can turn off the outputs, for instance, in case of a fault condition that lasts more than a given time interval. When no measurements are required, the microcontroller and ADC can be set to power-down mode, so that all clocks are stopped and no digital disturbance can be generated whatsoever. The microcontroller is automatically awakened from power-down if an overload condition occurs at the outputs. If this add-on card is not connected, the rest of the circuit is still operational, although with the last output voltage setting and without the additional functionalities that the digital board provides.

III. CURRENT LIMITING AND THERMAL FOLDBACK PROTECTION

Figure 6 shows the schematics of the DRIVER, TEMP, and LIMIT blocks in more detail. The schematic shows only the positive side; the negative side is identical, with all N-type transistors replaced by their P-type counterparts and vice versa.

The output of the DRIVER block is filtered with a 2200 µF electrolytic capacitor, with a 5.6 Ω resistor in series to compensate the pole above about 10 Hz. Other capacitors are typically connected at the output, close to the load. They are compensated with a high frequency zero by the series resistance of the connecting wires to the load. To guarantee stability at low frequency even in case of highly capacitive loads, the series combination of 100 kΩ and 100 nF was placed in the feedback loop of A3. Above about 15 Hz, the 100 kΩ resistor, together with the 1 kΩ resistor in series with the input, limits the gain of A3 to 100. The effect is to increase the bandwidth of A3, moving the phase shift due to the dominant pole of the opamp to a higher frequency.

The 10 Ω resistor and 10 µF capacitor between the gate and source of $M_P$ set another pole and a zero in the feedback loop, decreasing the loop gain and ensuring stability at high frequency. At the same time, the fact that the capacitor is connected to the source of $M_P$ and not to ground results in a higher power supply rejection ratio (PSRR) at high frequency. In fact, any disturbance injected at high frequency at the source of $M_P$ is directly injected also at the gate, preventing its propagation...
Implementations have been proposed in recent years.\textsuperscript{10,11} Circuits can be found in the literature, and new design implementations have been proposed in recent years.\textsuperscript{12–14} An example can be found also in a previous version of the present circuit.\textsuperscript{7}

When a foldback protection is engaged, a positive feedback loop is formed: as the current limit is reduced to limit the power in the output transistor, the output voltage decreases, which further reduces the current limit. A common drawback with a classic foldback is a possible lock-out condition, where the protection remains engaged even when the critical condition that triggered the protection (for instance, a short to ground at the output) is removed. An external reset is needed in that case to restore the proper operating conditions. A classical foldback protection can also be unduly triggered at switch-on, when the system must supply a large peak current to the load while increasing the output voltage from 0 V.

In the present circuit, a different kind of protection against overheating was designed. The TEMP block compares the temperature of the power transistor, measured by the silicon diode $D_{t}$ mounted very close to $M_{P}$, with ambient temperature, measured by an identical diode $D_{A}$ located away from $M_{P}$. Both diodes are BC858 bipolar transistors in SOT-23 package. The difference in the forward voltage drop of the two diodes is proportional to their temperature difference multiplied by 2.1 mV/°C. The voltage difference is amplified and used to generate a current that is proportional to the temperature difference. The current is sent to the LIMIT block to offset the voltage at the base of $Q_{2}$. As the temperature of the power transistors rises, for instance, as the consequence of a protracted overcurrent condition, then the output current limit is decreased from 6 A to lower values. A negative thermal feedback is established: reducing the maximum output current reduces the power consumption and effectively limits the maximum temperature that the output transistor can reach, under any circumstance, regardless of the voltage drop across it. The maximum temperature that can be reached corresponds to the condition where the current limit goes to zero, which happens when the current from the TEMP block alone generates a 600 mV drop at the base of $Q_{2}$.\textsuperscript{9}

$$T_{\text{MAX}} = T_{\text{AMB}} + \frac{600 \text{ mV}}{21 \text{ V/V} \times 2.1 \text{ mV/°C} \times 15 \text{ kΩ}} + \frac{15 \text{ kΩ}}{2.2 \text{ kΩ}}$$

$$\approx T_{\text{AMB}} + 90 \degree \text{C}.$$ (1)

where $T_{\text{AMB}}$ is ambient temperature, and 21 V/V is the gain of the amplifier in the TEMP block. In our case, we expect the ambient temperature inside the electronic crates to be around 40 °C–50 °C. The maximum temperature of the power transistors allowed by the circuit is then about 130 °C–140 °C. The dominant pole of the thermal feedback loop is the thermal inertia of the power transistors, which depends on the quality of the thermal conduction to the heat sink. Stability is ensured

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**FIG. 6.** Schematic of the output stage and protections (positive side only).
since in any case, even in case of very poor connections to the heat sink, the thermal dynamics are much slower than all the other electronic time constants. This mechanism essentially provides a foldback protection that is free of unwanted lock-out phenomena. At switch-on, assuming that the output transistor is at room temperature, the system is able to supply a large peak current, up to 6 A. The foldback protection is only engaged as soon as the temperature of the output MOS rises above the safety level.

Figure 7 shows the output voltage, the output current, and the temperature of the output transistor versus time, while the output was repeatedly shorted to ground. At the beginning of the measurement, the circuit was operating without load: the output voltage is 5 V and the current is 0 A. The temperature of the output transistor is about 27 °C. After about 30 s the output was shorted to ground. The peak current is 6 A at first, but as the temperature of the output transistor rises, the output current promptly reduces to lower values, slowing the temperature rise. By looking at the exponentials, one would expect the system to eventually stabilize to a condition where the temperature of the output transistor is about 100 °C and the output current is limited to about 3 A. The temperature value is compatible with what is set by Equation (1), considering that the ambient temperature is now 27 °C. At 50 s the short was removed: the current falls back to zero, while the temperature of the output transistor relaxes to lower values.

At about 100 s the heat sink on the power transistor was removed. The output was then again shorted to ground. The evolution is similar to the first time, aside from the fact that the temperature is now rising faster, since the heat sink was removed, and the current is now being limited to less than 2 A. While all this happens, the microcontroller on the digital add-on board is monitoring the voltages and currents. It is programmed to cut off the output if the short condition lasts for more than 30 s. At about 150 s this additional protection engages the following: the output is disabled by the microcontroller, and both voltage and current go to zero. At this point the output stays disabled until a proper command is received by the microcontroller via CAN bus. In the meantime, the microcontroller continues to monitor the recovery of the temperature of the output transistor towards ambient temperature.

IV. NOISE MEASUREMENT

The setup used to measure the noise is shown in Figure 8. The two symmetrical output voltages $V_P$ and $V_N$ of the device under test (DUT) were set to ±5 V. No dependency of the noise performance on the output current was observed; therefore, all the following measurements were taken with 1 A loads to ground. The two outputs were also connected to a resistive divider made of four precise Vishay SMR1DZ foil resistors of values 250 Ω and 2 kΩ, as shown in Figure 8. The middle point of the divider where the noise measurement is performed is at 0 V and was DC coupled to the amplifier, an OP27 operational amplifier from Analog Devices, operated with a gain of 101 and a bandwidth of 80 kHz. Its output was AC coupled with a 10 μF 63 V Vishay Roederstein Polyester (PET) capacitor to the input of an Agilent 35670A spectrum analyzer (1 MΩ to ground). The noise of the amplifier and of the resistive divider referred to the nodes marked as $V_P$ or $V_N$ is 40 nV/√Hz at 0.1 Hz, 15 nV/√Hz at 1 Hz, 10 nV/√Hz white and was subtracted quadratically from all measurements.

Two large capacitors $C$, both made of the parallel combination of a 15 000 μF 25 V electrolytic, a 8200 μF 16 V electrolytic, and a 10 μF 63 V PET capacitor, are used together with the switch $SW$ to filter the positive or the negative side above 0.03 Hz, allowing to measure the noise of the unfiltered side. In order to make sure that there was no noise coming from the leakage current of the large electrolytics, the noise measurement was performed also with both sides filtered, observing no significant difference with respect to the case where the input of the amplifier was at ground.

Leaving both sides unfiltered allows to measure the noise of the sum $V_P + V_N$. This cancels the anticorrelated part of the noise, that is, the part that originates in the VREF block and is therefore present at the same time on both outputs, with opposite signs. What is left in $V_P + V_N$ is the uncorrelated part of the noise of $V_P$ and $V_N$, which comes from the DRIVER blocks. Being the sum of two identical but independent sources, it adds in power to give a noise $\sqrt{2}$ times higher. In the following plots, the noise spectra of $V_P$ and $V_N$ are shown together with the noise spectra of $(V_P + V_N)/\sqrt{2}$ to make the amount of correlation in the noise of $V_P$ and of $V_N$ clear at a glance. The noise performance was evaluated for three slightly different versions of the circuit. The differences are in the choice of low pass filters inside the FILTER blocks and of the operational amplifiers in the DRIVER blocks.

The schematic and the noise spectrum of the first version of the circuit is shown in Figure 9. The operational amplifier is an ADA4084, with BJT input stage. The cutoff frequency of the FILTER block is 16 Hz. The input current of the amplifier (140 nA typical) prevents the use of a resistor larger than 1 kΩ in the filter, to avoid additional noise and drift. The

![FIG. 7. Output voltage, output current (both on the left y-axis), and temperature of the output transistor (right y-axis) versus time in case of shorts at the output.](image1.png)

![FIG. 8. Setup for noise measurements with the spectrum analyzer. The device under test and the amplifier are located in a Faraday cage to shield from external disturbances.](image2.png)
capacitor is a 10 μF 63 V Vishay Roederstein PET capacitor (MKT1820 series). Electrolytics and large value ceramics have non-negligible leakage when biased with a DC voltage. PET capacitors on the contrary ensure a negligible leakage, but values larger than 10 μF are unpractical to fit on a PCB. The noise of $V_P$ and $V_N$ above the cutoff is about 20 nV/√Hz, dominated by the ADA4084 in the DRIVER block, operating with a gain of two since the outputs are set to 5 V. Below the cutoff frequency the noise is larger, just below 100 nV/√Hz at 1 Hz, due to the additional contribution coming from the ±2.5 V reference voltages. This is confirmed by the measurement of the noise spectrum of $(V_P + V_N)/\sqrt{2}$ that is lower than that of $V_P$ and $V_N$ below the cutoff frequency.

In order to improve the filtering of the reference voltages at low frequency, a dedicated passive filter was applied. Its schematic and the resulting noise spectrum are shown in Figure 10. The filter is now composed of two parts. The first is an RC low pass composed of a 220 μF resistor and a 2200 μF 25 V aluminium electrolytic capacitor, with a cutoff at 0.3 Hz. The capacitor is biased at 2.5 V, but its leakage current does not affect the precision of the reference voltage, since the leakage current flows through the 220 Ω resistor. The other part is again a low pass composed of a 10 kΩ resistor and a 100 μF 16 V ceramic capacitor, but the capacitor is biased at 0 V and thus does not show leakage. This solution allows to prevent the leakage current of large value capacitors from affecting the output drift. The leakage current of the 2200 μF capacitor however can also generate current noise, especially at low frequency, which becomes a voltage noise source across the 220 Ω resistor. Therefore to avoid injecting low frequency noise through the 100 μF capacitor, the 220 Ω resistor cannot be increased to a larger value. Since the input current of the operational amplifier now passes through a 10 kΩ resistor, the device was replaced with a CMOS-input amplifier, the OPA2188, having a smaller input current. The OPA2188 is a zero-drift (chopping) amplifier. Although, due to their operating principles, zero-drift amplifiers can show excess noise at high frequency (hundreds of kHz), none was found in our case, since the output of the DRIVER block is well filtered at high frequency. The noise spectra of Figure 10 show a considerable improvement in the output noise at 1 Hz, which is now 50 nV/√Hz. The output noise is now entirely due to the DRIVER blocks, its main contributor being the operational amplifier. The OPA2188 used here has a higher white noise than the ADA4084, hence the white noise at the output is now 30 nV/√Hz. The noise at 0.1 Hz is unchanged and still shows some degree of correlation between $V_P$ and $V_N$, since it is below the cutoff frequency of the FILTER block. Due to the smaller unity gain bandwidth of the OPA2188 (2 MHz) compared to the ADA4084 (10 MHz), the circuit now shows a closed loop bandwidth limit of 2 kHz, with a small peak just before the roll-off.

In order to improve the noise performance at high frequencies, the operational amplifier was replaced with a JFET-input device, the OPA2140, without modifying the FILTER block. The resulting spectra are shown in Figure 11. Noise is 50 nV/√Hz at 1 Hz and 20 nV/√Hz white, mostly uncorrelated between $V_P$ and $V_N$. The resulting total noise from each output between 0.1 Hz and 10 Hz is 125 nV RMS, or 0.8 μV peak to peak. If a bandwidth up to 100 Hz is considered, the total noise is 240 nV RMS, or 1.6 μV peak to peak. A small degree of anticorrelation is evident at 0.1 Hz, where some noise is contributed by the VREF block. This version of the circuit provides the best noise performance. Using the OPA2140 comes with a minor drawback: it needs at least 3.5 V between the inputs and the positive supply rail, resulting in our case in a minimum supply voltage requirement of 6 V.

The noise measurements presented here are in a perfect match with what can be calculated from the noise spectra given in the datasheet of the components used in the circuit. The measurements were repeated on a few samples, obtaining consistent results. For this reason, the noise characterization was performed only on a few samples, and not on the entire production lot.
FIG. 11. Noise spectra of the circuit, version 3. Same as version 2, but with a different opamp in the DRIVER block, resulting in lower noise and wider bandwidth.

V. DRIFT AND CALIBRATION

Thanks to the choice of components used in the circuit, the typical thermal drift of the boards before calibration is already in the ppm/°C range, with a 0 ppm/°C minimum around room temperature. To improve the performance further, and to shift the minimum to the expected operated temperature of about 45 °C, all the boards were tested and calibrated. Here the results on the first 30 boards are presented. The circuits were placed one at a time in a Votsch VT 7004 climatic chamber. The measurements were performed with the outputs set at ±5 V and with 1 A loads. The DC voltages were measured with 1 µV resolution with a Keithley 3706A 7½ digit multimeter. Since the voltages were measured at the sense node of the Kelvin connection to the output load, no significant dependence on the output current was observed.

In a first run, each circuit was measured at 40 °C and 50 °C, in order to determine its drift at 45 °C, the expected operating temperature of the boards. The drift found on 30 boards at 45 °C was (1.7 ± 1.4) ppm/°C at the positive output and (1.0 ± 2.0) ppm/°C at the negative output (errors quoted as ±2σ).

The circuit used to calibrate the output voltage is shown in Figure 12. The drift correction was performed by injecting a small current proportional to temperature at the non-inverting node of the operational amplifier in the DRIVER block. The correction current is derived from the voltage across the forward biased diodes $D_1$ or $D_2$, providing the well known voltage coefficient of ±2.1 mV/°C, depending on the sign of the correction needed. The diodes were biased using a ±4.5 V reference, generated on board using adjustable low-dropout regulators LT3085 from Linear Technology and TPS7A30 from Texas Instruments. The value of resistors $R_{D1}$ or $R_{D2}$ was selected to obtain the required amount of drift correction for each board. To correct a positive drift $X$ expressed in ppm/°C, $R_{D2}$ was left open, and the value of $R_{D1}$ was chosen as

$$R_{D1} = \frac{R_{G2} \cdot 2.1 \text{ mV/°C}}{X \cdot 2.5 \text{ V}}. \tag{2}$$

To correct a negative drift, $R_{D1}$ was left open, and Equation (2) was used to calculate the value of $R_{D2}$. Since $R_{G2} = 1 \text{kΩ}$, the

FIG. 12. Schematic of the circuit that generates the correction currents used for calibration. Identical and independent circuits are used on the positive and negative sides.

FIG. 13. Absolute value of the output voltages versus temperature after calibration, for the 30 boards produced. Dashed lines corresponding to ±1 ppm/°C are shown at the bottom for comparison. The drift close to the expected operating temperature (45 °C) is below ±1 ppm/°C after calibration. The absolute value is in all cases within ±350 µV (±70 ppm) from the target value of 5 V.

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values of $R_{D1}$ or $R_{D2}$ needed to correct a drift of a few ppm/°C are in the range of a few hundred kΩ, and the corresponding currents are of the order of 10 µA. The values of $R_{C1}$ or $R_{C2}$ were then selected to tune the absolute value of the output voltage, by injecting a positive or negative current. $R_{C1}$ was used to compensate the offset due to $R_{D2}$, while $R_{C2}$ was used to compensate the offset due to $R_{D1}$. Identical (and independent) correction circuits were used to calibrate the positive and the negative outputs.

The regulators used to generate the ±4.5 V references show temperature drifts below ±50 ppm/°C between 0 °C and 75 °C. Since the values of $R_{C1}$ or $R_{C2}$ are in the hundreds of kΩ range, such drift is attenuated by at least a factor of 100 before reaching the outputs. The additional contribution is then well below ±0.5 ppm/°C and can be neglected. The same can be said about the noise injected by the correction circuits: since the noise of the ±4.5 V references is at the level of 100 nV/√Hz down to low frequency, this contribution is reduced below 1 nV/√Hz at the outputs and becomes negligible.

After the proper values of the correction currents were set, the circuits were again one at a time placed in the climatic chamber, and the temperature was swept from 20 °C to 60 °C in 10 °C steps, to check the success of the calibration procedure. The resulting measurements are shown in Figure 13. The output voltages at 45 °C are all within ±350 µV from the nominal values of ±5 V, corresponding to a maximum absolute error of ±70 ppm. The drift at 45 °C is now (−0.2 ± 0.8) ppm/°C at the positive output and (−0.1 ± 0.6) ppm/°C at the negative output. The comparison between the measured drift at 45 °C before and after calibration is shown in Figure 14.

VI. CONCLUSIONS

The design and characterization of a low noise and high precision linear power supply was described in this paper. To protect the output MOSFETs against overcurrent or overheating, the circuit uses an original analogue foldback scheme, based on the direct measurement of the temperature of the output transistors. Accurate design choices and filtering resulted in a measured noise of 50 nV/√Hz at 1 Hz and 20 nV/√Hz white when the output is set to ±5 V, corresponding to 125 nV RMS (0.8 µV peak to peak) between 0.1 Hz and 10 Hz, and 240 nV RMS (1.6 µV peak to peak) between 0.1 Hz and 100 Hz. The PSRR of the circuit at low frequency is about 100 dB. A proper compensation of the output driver gives a PSRR larger than 40 dB up to high frequency. A thermal drift of a few ppm/°C was measured before calibration. A simple calibration procedure allowed to reduce it below ±1 ppm/°C and to obtain an absolute precision of ±70 ppm, or ±350 µV at ±5 V. The performance of the circuit makes it suitable to supply stable and low noise voltages to power front-end circuitry in sensitive experiments at the frontier of particle physics.