A SUGGESTION FOR THE RICH FRONT-END READOUT

Front-End Electronics (linear)

We are suggesting a scheme for the front-end electronics (FEE) of the RICH detector. The simplified diagram is shown in Figure 1. A Charge Sensitive Preamplifier, CSP, reads the detector signal. Its output feeds a shaper, realized with a RC-CR filter. After the Shaper Filter, a Sample and Hold, S/H, holds the peak value of the shaped signal. A multiplexed differential output buffer is able to drive a twisted cable to the acquisition circuit.

The S/H and the multiplexer are fired following two possible solutions.

1. A comparator triggers the S/H when the input signal exceeds a suitable threshold. This is possible as the signal peak at the shaper output appears well after the output of the CSP has made the full excursion. After locking the peak of the signal, the S/H can be reset in two ways.
   A) - Auto-reset, which happens when the CSP output has become small enough: this is verified after the peak has been reached. This condition assures that the S/H is ready for a new acquisition even if the main trigger has not been asserted.
   B) - When the main trigger is asserted, it resets the S/H after having generated the multiplexing command. The main trigger can be implemented on a single line, with a toggle effect: multiplexing and reset.

2. The main trigger regulates both the S/H operations and the multiplexing. In this case the comparator needs not to be present, or, if present, can be put in the OFF state for safe power consumption (by operating on the switches \(\gamma\)'s).

We prefer the first solution.

Power consumption of the proposed scheme can be limited to be less than 1 mW/channel for a shaping time not smaller than 1 \(\mu\)sec.

Readout Control Logic (digital)

We propose the following readout scheme, based on a group of 16 FEE channels and 1 local Readout Control Logic (RCL), dedicated to the 16 channels. The Master Trigger Control Signal (MTCS) is issued to RCL in the form of a train of 16 pulses. It is derived from the AMS master trigger with some delay to allow the S/H to reach the peak. The leading edge of the first pulse of MTCS initiates a gate signal, that keeps the S/H locked until the trailing edge of the last 16th pulse that resets the gate signal. Each pulse increments a binary counter-decoder, driving the multiplexer (MUX) that selects the 16 channels one at a time. The output of the MUX is fed to the output buffer, driving the bipolar line.

At the receiving end of the bipolar line the DAQ gets the output in coincidence with the MTCS pulses, therefore it knows the address of each channel of each PMT.

The RCL is made in CMOS technology, directly on the same chip where the 16 channel are located. In absence of MTCS the power consumption of RCL is less than a \(\mu\)watt.
Figure 1: Simplified schematic diagram of the very front-end for RICH detector.