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Many thanks for your assistance.
We describe the criteria for the selection of the input transistor of the very front-end for the detector, an array of 988 macro bolometers. Each of such macro bolometer is composed of a crystal of TeO₂, having a mass of 750 g, to which a thermistor is glued. Due to the very large mass of the crystals, the detector response time is very slow and limited to a few Hz. The quoted characteristic for the CUORE (Cryogenic Underground Observatory on Rare Events) detectors make it attractive a solution based on a complete room temperature operated front-end. The very important requirements of such a solution are a very small parallel and low frequency series noise. We worked to the selection of a Si JFET having a gate area and pinch-off voltage that fulfil the CUORE requirements. The selected JFET has an input gate current of less than 60 fA at 40°C (the expected operating temperature at regime). The noise at 1 Hz is about 3 nV/√Hz at the operating point of $I_{DS}$ of 0.5 mA and $V_{DS}$ of 0.5 V, selected for having small power dissipation. Thanks to the quoted results the limit in the energy
resolution given by the preamplifier is about 10 times better than that presently achievable by the crystals tested and candidate for CUORE. The wafer from which the semi-custom JFET has been cut was previously probed. All the production consisting of 1200 JFETs pairs is already available.

Keywords

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The Design of the Input Stage for the Very Front-End of the CUORE Experiment

Claudio Arnaboldi · Gianluigi Pessina

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Abstract We describe the criteria for the selection of the input transistor of the very front-end for the detector, an array of 988 macro bolometers. Each of such macro bolometer is composed of a crystal of TeO$_2$, having a mass of 750 g, to which a thermistor is glued. Due to the very large mass of the crystals, the detector response time is very slow and limited to a few Hz. The quoted characteristic for the CUORE (Cryogenic Underground Observatory on Rare Events) detectors make it attractive a solution based on a complete room temperature operated front-end. The very important requirements of such a solution are a very small parallel and low frequency series noise. We worked to the selection of a Si JFET having a gate area and pinch-off voltage that fulfils the CUORE requirements. The selected JFET has an input gate current of less than 60 fA at 40°C (the expected operating temperature at regime). The noise at 1 Hz is about 3 nV/$\sqrt{\text{Hz}}$ at the operating point of $I_{DS}$ of 0.5 mA and $V_{DS}$ of 0.5 V, selected for having small power dissipation. Thanks to the quoted results the limit in the energy resolution given by the preamplifier is about 10 times better than that presently achievable by the crystals tested and candidate for CUORE. The wafer from which the semi-custom JFET has been cut was previously probed. All the production consisting of 1200 JFETs pairs is already available.

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1 Introduction

In the design of the very-front end of a detector the very critical part is the input transistor, which limits the Signal to Noise ratio, S/N. This applies in particular to the case of bolometers.

We present the criteria we have used to select the input transistor of the very front-end for the CUORE detectors. CUORE is an array of 988 macro bolometers. Each of such macro bolometer is composed of a crystal of TeO$_2$, having a mass of 750 g, to which a Nuclear Transmutation Doped, NTD, Ge thermistor is glued. Due to the very large mass of the crystal the detectors response time is very slow, limited to a few Hz. A typical signal has a rise time of about 50 ms and a fall time constant larger than a few hundreds ms. The impedance of the NTD thermistors at the operating point, about 10 mK, is in the 100 MΩ range. The quoted characteristic for the CUORE detectors make it attractive either a solution based on a cold stage followed by a room temperature second stage, or a solution based on a complete room temperature operated front-end. This is possible because even a large capacitance of the electrical connecting link, of a few hundred pF, gives a negligible deterioration of the S/N. We have already shown [1] that it is possible to develop a differential buffer cold stage showing a sub μW power dissipation, resulting in less than 5 mW of total dissipation for the whole CUORE array. In this set up the load resistors need to be at cold and every detector requires 4 wires from the room temperature, 2 for the differential bias voltage and 2 for the differential readout. In case the front-end is room temperature operated only 2 wires are needed to every detector, since the load resistors may be located at room temperature, too. This second solution is very attractive since the saving in a factor of two in the number of the connecting wires inside the fridge. The input stage of a room temperature operated front-end has the very important requirement of a very small parallel noise. In addition, the series noise must be very low at low frequency in CUORE. We worked in selecting a Si JFET having a gate area and pinch-off voltage that fulfils the CUORE requirements.

In the following sections we will show the selection criteria and the experimental results.

2 Front-End Readout Requirements

The readout of a bolometric detector finds a natural solution with a cold first stage, to minimize signal integration due to the parasitic electrical capacitance of the connecting leads. A unity gain follower stage is adopted with a pair of load impedances at cold, Fig. 1. The differential readout is preferred to reduce the cross-talk between channels and the main-line disturbances. Every detector is connected with 4 wires: 2 for the load resistors biasing (every detector needs a dedicated bias) and 2 for the signal readout, at the sources of the JFETs. One additional wire (the dashed one in Fig. 1) is shared among different channels for the biasing of the drains of the JFETs.

If the detector signal bandwidth is of few Hz, as is the case for large mass crystals, the acceptable electrical parasitic capacitance can be large. In this situation, another very attractive solution is a front-end having the first stage at room temperature. By
locating the load resistors at room temperature, only two wires are enough to readout the thermistor, Fig. 2. The saving of a factor of two in the detectors wiring allows the minimization of the heat injection, a very important challenge in CUORE, which will consist of 988 channels.

A moderate electrical capacitance value of about 300 pF can be obtained across a link having a length of less than 4 m. The noise of the room temperature front-end must have a very low value for both the series component as well as the parallel component. Parallel noise has two main contributions: the Shot noise of the input current of the front-end and the thermal noise of the load resistors. Series noise is given by the front-end only. We have addressed these three noise sources.

### 3 JFET Selection and Measurements

#### 3.1 Parallel Noise

The value of the dynamic impedance of our bolometers makes the parallel noise the main source to be minimized. The series combination of the two load resistors $R_L$ of Fig. 2 has a value of 54 GΩ and gives a parallel noise at the margin of our specifications, as it will be shown below. Low frequency noise, LFN, of $R_L$ was made negligible by design [2]. We tried to select a JFET transistor able to add a very marginal contribution.

In a JFET the input current is due to the reverse bias of the gate with respect to the source, $V_{GS}$, and to the drain, $V_{GD}$, channel terminals. As known, the level
of the applied reverse bias modulate the width of the depletion region, hence the channel volume to which the drain current is proportional. The input parasitic current has two contributions [3, 4]. The first is the diffusion current at the junction. It is given by the thermal generation of the (minority) holes inside the channel and is proportional to the square of the intrinsic concentration, \( n_i^2 \), from the mass action law.

The diffusion current is almost independent on the amount of bias. The second term is the Generation Recombination, G-R, current inside the depletion region. It derives by the presence of trapping centres. Its magnitude is proportional to the concentration of the trapping centres and on \( n_i \), via the mechanism that gives rise the statistic of the recombination [3, 4]. The magnitude of this current depends on the depletion region width and is bias dependent. The smaller the volume of the depletion region the smaller is the G-R current.

\( n_i^2 \) is proportional to the exponent of \( \frac{E_G}{K_B T} \), therefore \( n_i \) to the exponent of \( \frac{E_G}{2K_B T} \), \( E_G \) being the energy gap of the semiconductor, \( K_B \) the Boltzmann constant and \( T \) the absolute temperature. The two currents have therefore a different behaviour with temperature. Often the G-R process dominates and the empirical formula used is the following:

\[
I_G \approx I_S(V) \exp\left(-\frac{E_G}{mK_BT}\right)
\] (1)

With the selected JFET, the semi-custom SNJ132287 pair from Interfet, (1) is satisfied with \( I_S = 0.653 \) A and \( m = 1.355 \). In (1) the reverse bias is the largest applied between \( V_{GS} \) and \( V_{GD} \), or \(-0.75 \) V. The value of \( m \) close to one is an indication that the G-R centres concentration is small. We therefore try to fit data with the theoretical expected behavior:

\[
I_G = I_{DIF} \exp\left(-\frac{E_G}{K_B T}\right) + I_{GEN}(V) \exp\left(-\frac{E_G}{2K_B T}\right)
\] (2)

In this case it resulted, with good fit of measurements, \( I_{DIF} = 8734 \) A and \( I_{GEN} = 28 \) \( \mu \)A. The results of the fit are shown in Fig. 3. Measurements have been carried out with the Semiconductor Analyzer Keithley 4200 while the device was inside an environmental chamber, Vötsch VC 4018, having the Relative Humidity, RH, control option. We can see that the RH has a slight, but non marginal, effect on the gate current measurements. At an RH of 10% the gate current, at a supposed working temperature of 40°C, is about 55 fA. This value, when RH is increased to 60%, becomes 65 fA. It has to be remarked that the added current does not generate shot noise.

Noise performances of the preamplifier can be calculated from Fig. 4. If the value of the load impedances, \( R_L/2 \), is much greater than that of the thermistor, only half of the current from any parallel noise source will flow through the thermistor, across which it will develop the differential preamplifier input voltage:

\[
V_{+G}^2 \approx 2 \times \left(2qI_G\right) \frac{|Z_B|^2}{4}
\]

\[
V_{+L}^2 \approx 2 \times \left(4K_B T \frac{2}{R_L}\right) \frac{|Z_B|^2}{4}
\] (3)

Each of the parallel sources of Fig. 4 has a counterpart on the other terminal to which, by symmetry, will add the same contribution. This is the reason of the factor
Fig. 3 (Color online) Gate current, $I_{GS}$, vs. temperature, $T$, at two different humidity conditions. The fits have been generated with the function in (2).

$\begin{align*}
I_{DS} &= 0.5 \text{ mA} \\
V_{DS} &= 0.6 \text{ V}
\end{align*}$

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Fig. 4 Preamplifier model for noise calculation. The noise sources in dashed represent the equivalent total noise model to be calculated.

2× in (3). The total equivalent parallel noise, the dashed generator $\overline{i_T^2}$ in Fig. 4, in parallel to $Z_B$ is, therefore:

$$\overline{i_T^2} \approx 2q \frac{i_G}{2} + \frac{4k_B T}{R_L} \quad (4)$$

The parallel noise of the differential preamplifier of Fig. 2, when at its input a SNJ132287 pair is used, can be estimated from (4) in 0.094 fA/$\sqrt{\text{Hz}}$, a very good figure, while the noise from the 54 GΩ load resistors is about 0.5 fA/$\sqrt{\text{Hz}}$.

The main reason for a so small parallel noise from the JFETs is the very good quality of the technological process. We have optimized further the results selecting the devices with a small pinch-off voltage and small $I_{DSS}$, the largest handled channel current, $I_{DS}$, minimizing the applied bias at the operating point. The graph on the left in Fig. 5 shows the static characteristics of the transistor. The pinch-off voltage is close to $-0.5$ V. In this condition, at the indicated bias of $I_{DS} = 0.5$ mA and $V_{DS} = 0.6$ V, an adequate performance is obtained, with a transconductance of about 5 mA/V. Fig. 5 graph on the right, and a gate to source voltage of about $-0.16$ V ($V_{GD} = V_{GS} - V_{DS}$ is $-0.76$ V). The input capacitance, measured with the procedure described in [5], is about 19 pF, of which about 8 pF is the gate to drain contribution.
3.2 Series Noise

The total differential series input noise $e_A^2$ of Fig. 4 is easily calculated in $2e_A^2$. Series gate noise from one JFET is shown in Fig. 6. The high frequency or white noise is given by the channel thermal noise, close to $4K_B T/\delta_{gm}$, $\delta_{gm}$ being the JFET transconductance, 5 mA/V. The LFN component is quite low, consistent with the very small level of G-R concentration verified in the gate current measurements. At 1 Hz the noise rises to about 3 nV/√Hz. In Fig. 6 the noise fit, from which the parameters have been extracted, is shown superimposed on the noise spectrum.

4 Front-End Contribution to the Resolution

The contribution of the preamplifier to the energy resolution is calculated with the optimum filter [6], whose algorithm is applied off-line in our acquisition system. The typical time constant that roll-off our detector signals is assumed to be about 300 ms,
on average. Due to the very small bandwidth of the detector signals the series preamplifier noise is assumed white with the value measured at 1 Hz. We have considered, as a worst condition, a detector dynamic impedance of 50 MΩ and a spread in the detector Energy Conversion Gain, ECG, that ranges between 100 μV/MeV and 500 μV/MeV. Under these assumptions the noise of the preamplifier corresponds to an energy resolution between 240 eV_{FWHM} and 50 eV_{FWHM}. If we include the parallel noise of the load resistors at room temperature, the performance rises from 1220 eV_{FWHM} to 250 eV_{FWHM}. This figure is adequate for the CUORE experiment where the energy resolution expected is larger than 1 KeV_{FWHM} only for the detectors having the larger ECG, becoming proportionally worse approaching the lower ECG.

References