A very simple method to measure the input capacitance and the input current of transistors

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Abstract

We describe a method to measure the gate capacitance and the gate current of transistors at any temperature and at any operating condition. Discrimination between the total input capacitance and transfer reverse capacitance (gate to drain capacitance) is also possible with high accuracy. With this data the optimization of the signal to noise ratio and power dissipation can be achieved in the design of the front-end electronics for nuclear applications. © 2001 Elsevier Science B.V. All rights reserved.

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1. Introduction

The major part of nuclear detectors are instruments that show very large dynamic impedance, often appreciable with a capacitance. The readout electronics for these apparatus must match such impedances, if the Signal to Noise ratio, $S/N$, must be maximized [1]. The input impedance of the open loop preamplifier, the first stage of the amplification of the detector signal, must be known with good accuracy to face this aim. Since the preamplifier has at its input an active device, the knowledge of its input impedance is derived from the characteristic of the input transistor at the selected operating point. The information that can be deduced from the data sheet provided with the device is generally not adequate since it describes the transistor characteristic at an operating condition which is very seldom close to the selected one. Device characterization is possible with the use of a network analyzer, but unfortunately it is not always possible to have available such an expensive instrument.

Nevertheless when the front-end for a detector of known impedance is to be designed, a pre-selection of the transistors having the suitable characteristic allows saving of project time. For this reason we have implemented a very simple, precise and low cost method for the measurement of the input impedance of any transistor.

Since the measurement procedure allows taking care of all the possible parasitic effects of the setup, it is possible to adopt this method also for the determination of the input capacitance of Junction
Field Effect Transistors (JFETs), when the transistors are put in a cryogenic environment. This is an invaluable feature for the design of the front-end electronics for bolometric detectors [2]. For this circumstance the power dissipation of the front-end readout, operated at cryogenic temperature, must be minimal and the transistors used for this purpose are forced to work at their extreme conditions, hence the knowledge of their actual parameters is of primary concern.

The suggested method also allows very low level characterizations of the input current of transistors. When characterizing JFETs at cryogenic temperature sub-fA level of leakage currents can be easily inspected.

In Section 2 a description of the requirements for a front-end electronics is reviewed, suggesting a method to optimize the $S/N$ ratio once the noise and the capacitance of the input transistor to be selected are known. In Section 3 the complete description of the measurement system and the experimental results are shown and compared to the specifications obtained from the data sheets. Finally, in Section 4 descriptions and results are given on the measurement of very small input currents of transistors.

2. The signal to noise ratio for a front-end readout

2.1. The readout for bolometric detectors

Bolometers are very sensitive detectors that operate at cryogenic temperatures, down to as low as 10 mK. They are able to reach high energy resolution, of the order of a few eV [3]. Their principle of operation is quite simple. On a dielectric crystal a temperature to electrical transducer is glued. As an example, in our case the transducer is a semiconductor thermistor [4]. When an energetic particle impinges on the crystal, it generates a temperature increase of the crystal itself that is inversely proportional to the crystal heat capacity, which is extremely low at a low temperature. The thermistor converts the temperature increase to a measurable electrical signal.

Semiconductor thermistors present a complex impedance with a positive, or inductive, imaginary part. The real part of such impedance is of a few tens of MΩ. Although the frequency bandwidth is limited to a few kHz at most for very small mass bolometers, the impedance that shunts the thermistor, due to parasitic capacitance and the front-end, must be selected to optimize $S/N$. This requirement asks for a location of the preamplifier as close as possible to the detector, at cryogenic temperature. The more common solution is to employ a Silicon JFET operated at its optimum temperature, between 100 and 150 K. To minimize power dissipation the configuration adopted is the unity gain common drain configuration, shown in Fig. 1. For the calculation of the $S/N$ we refer to Fig. 2. There the bolometer is approximated with its high frequency dynamic impedance, the resistance $R_B$, while the time dependence of the detector signal current, $i_B$, accounts for the actual detector response

$$i_B \approx \frac{K}{1 + s \tau_B} E,$$

(1)

$K$ being a normalizing factor, $E$ the particle energy and $\tau_B$ is the time constant that accounts for the...
detector signal and \( s \) is the complex angular frequency, \( s = j\omega \).

A parasitic capacitance \( C_p \) shunting the bolometer has been included in Fig. 2. The input capacitances of the JFET \( C_{GS} \) and \( C_{GD} \) are put into evidence. The detector noise is represented by the parallel generator \( \tau_B \), while the series noise of the JFET is \( \epsilon_j^2 \). In the first approximation both noise sources will be considered white. Eventually a low frequency contribution to the noise can be taken into account by a numerical solution [5]. The parallel noise of the cold JFET has been neglected, being very low at these temperatures.

If we assume the transconductance \( g_m \) of the JFET to be much larger than the conductance of the biasing resistor \( R_s \), the signal at the output, invariant in shape, in the frequency domain is given by

\[
V_{OUT}(\omega) = S(\omega)E = \frac{KE}{1 + s\tau_B} \frac{R_B}{1 + s(C_P + C_{GD})R_B}. 
\]

By neglecting the presence of the high frequency transition pole of the JFET, \( g_m/(C_{GS} + C_{GD}) \), the noise at the output results in

\[
\frac{V^2_{ONT}(\omega)}{\omega^2} = \frac{\omega^2(C_P + C_J)^2 R_B^2 \tau_B}{1 + \omega^2(C_P + C_{GD})^2 R_B^2} + \frac{\epsilon_j^2}{C_J - C_{GD}}. 
\]

From the above equations we see that the noise depends on the sum of the total value of the JFET input capacitance, \( C_J \), and parasitic capacitance \( C_P \), while the time dependence of the output signal depends on the sum of the transfer reverse capacitance \( C_{GD} \) and \( C_P \).

The square of the \( S/N \) at a selected measurement instant \( \tau_m \) is then given by, considering a unilateral expression for the noise spectrum

\[
\frac{S^2}{\mathcal{N}} = \frac{\left(1/2\pi \int_0^{+\infty} S(\omega)e^{j\omega \tau_m} d\omega \right)^2}{1/2\pi \int_0^{+\infty} V^2_{ONT}(\omega) d\omega}. 
\]

By applying the Schwartz inequality [1] to the numerator of Eq. (4) it is very easy to show that the \( S/N \) is in any condition limited by

\[
\frac{S^2}{\mathcal{N}} \leq 4 \frac{1}{2\pi} \int_0^{+\infty} \left( \frac{E^2|S(\omega)|^2}{V^2_{ONT}(\omega)} \right) d\omega. 
\]

In the above equation term 4 in the numerator comes as a consequence of considering the noise spectrum as unilateral. Consequently for the energy resolution it is valid that

\[
\Delta U_{RMS}^2 \geq \left\{ \frac{4}{2\pi} \int_0^{+\infty} \left( \frac{|S(\omega)|^2}{V^2_{ONT}(\omega)} \right) d\omega \right\}^{-1}. 
\]

The equal sign in the above two equations is valid when an optimum processing filter is used at the JFET output [6,7].

By including Eqs. (2) and (3) in Eq. (6) we obtain

\[
\Delta U_{RMS}^2 \geq \left\{ \frac{4}{2\pi} \int_0^{+\infty} \left[ \frac{(KR_B)^2}{1 + \omega^2 \tau_B^2} \times \frac{1}{\omega^2(C_P + C_J)^2 R_B^2 \epsilon_j^2 + R_B^2 \tau_B^2 + \epsilon_j^2} \right] d\omega \right\}^{-1}. 
\]

The calculation of the integral of Eq. (7) has been made by taking into account the technique of putting transistors in parallel when discrete transistors are used [8], or, equivalently, optimize devices area when the monolithic technology is available [9,10]. If the series noise measured for a given kind of transistor biased with a drain current \( I_{DS} \) is \( \epsilon_j^o \) and its input capacitance is \( C_o \), then any new transistor having an input capacitance \( C_J \), obtained by paralleling many such kinds of transistors, each one biased with \( I_{DS} \), will have a noise given by

\[
\epsilon_j^o = \frac{C_o}{C_J} \epsilon_j^o. 
\]

The inclusion of Eq. (8) in Eq. (7) results in

\[
\Delta U_{RMS}^2 \geq \frac{1}{K^2} \frac{1}{R_B^2} \frac{\tau_B^2 \sqrt{\left( \frac{\epsilon_j^o C_o + R_B C_J \tau_B^2}{C_J} \right) + (C_P + C_J) R_B \sqrt{\epsilon_j^o C_o}}}{C_J} \times \frac{1}{\sqrt{\epsilon_j^o C_o + R_B C_J \tau_B^2}}. 
\]
As can be seen in Eq. (9) \( \Delta U_{\text{RMS}}^2 \) increases if the JFET input capacitance \( C_J \) tends to a negligible or large value; an optimum exists for \( C_J \). Minimization of \( \Delta U_{\text{RMS}}^2 \) with respect to \( C_J \) is found by equating to zero the first derivative of Eq. (9), that results in

\[
\frac{C_J(C_J - C_P)}{C_0^2} = 2 \left[ \frac{\tau_B}{C_0 R_B} \sqrt{1 + \frac{R_B^2 \tau_B^2}{C_0^2 C_P + C_0}} \right] \times \left( \frac{C_0}{R_B^2 \tau_B} \right). \tag{10}
\]

The exact solution of the above equation for the capacitance \( C_J \) is not trivial. Nevertheless when dealing with bolometers it results that the time constant \( \tau_B \), hundreds of \( \mu \)s to ms for \( \mu \)-bolometers, is much greater than \( C_0 R_B \), so the value of \( C_J \) to satisfy Eq. (10) is sufficiently large, and the approximation becomes valid

\[
\frac{C_J}{C_0} \approx \sqrt[3]{\frac{2 \tau_B}{C_0 R_B} \left( \frac{C_0}{R_B^2 \tau_B} \right)^2} \tag{11}
\]

Eq. (11) says how many samples, given by \( C_J / C_0 \), of transistors of the selected technology should be put in parallel to maximize \( S/N \). The ratio \( C_J / C_0 \) depends on the measured noise \( \epsilon_o^2 \) as well as the input capacitance \( C_0 \) itself. It is therefore evident that it is important to know the value of the input capacitance of the transistor for bolometric applications.

2.2. The readout for capacitive detectors

Many types of ionization detectors show dynamic impedances that can be approximated with a capacitance. The scheme for a quite classical front-end realization, the Charge Sensitive Pre-amplifier (CSP) configuration, is shown in Fig. 3. The detector is now represented by the signal generator \( i_B \), a \( \delta \)-like current pulse, by its parallel noise, \( \overline{\epsilon_B^2} \), and by its dynamic impedance, the capacitance \( C_P \). The CSP is modeled with a dominant pole, single ended input amplifier having a JFET as the input transistor. Again the capacitances that characterize the JFET input and the series noise are put into evidence. Parallel noise has been considered negligible.

By assuming the feedback resistance \( R_F \) to be very large, and \( i_B = K E \delta(t) \) we get

\[
V_{\text{OUT}}(\omega) = S(\omega) E = \frac{K E}{\omega C_f}, \tag{12}
\]

while the noise at the output will be

\[
V_{\text{OUT}}^2(\omega) = \overline{\epsilon_B^2} + \omega^2(C_D + C_f + C_J)^2 \epsilon_o^2 \frac{1}{\omega^2 C_f^2}, \tag{13}
\]

Hence from Eq. (6):

\[
\Delta U_{\text{RMS}}^2 \approx \left\{ \frac{4}{2\pi} \times \int_0^{+\infty} \left[ K^2 \frac{1}{\omega^2(C_D + C_f + C_J)^2 \epsilon_o^2 + \overline{\epsilon_B^2}} \right] d\omega \right\}^{-1}. \tag{14}
\]

Eq. (14) coincides with Eq. (7) when \( \tau_B \) is zero and \( R_B \) is infinite and it is considered that \( C_P = C_D + C_f \). This proves that the adoption of a voltage sensitive preamplifier or a CSP has the same effect on the overall noise performance of an ionization detector. Even for the CSP case there will be an optimum for the transistor area, which can be determined by solving the integral of Eq. (14) and deriving with respect to \( C_J \). The result coincides with those shown in Eq. (10) provided the two positions \( \tau_B = 0 \) and \( R_B = \infty \). This gives \( C_J = C_D + C_f \) (a second solution, \( C_J = 0 \), does not result in a minimum but in an asymptote) proving again the importance of an accurate knowledge of the input capacitance of the transistor used.
3. The method to measure the input capacitance of transistors

It has been shown in the previous section that it is important to know the value of the input capacitance, at the selected biasing condition, for the transistor that directly faces the detector in the readout. We can see now how this capacitance can be measured easily and accurately.

A set up to be created to measure the input capacitance of a transistor in any condition of biasing and temperature must satisfy a few stringent requirements. It has to be constituted by a very sensitive probe that is allowed to be calibrated to cancel any possible parasitic effect. If necessary the discrimination between the total input capacitance and the transfer reverse capacitance of the transistor under measurement must be permitted.

A very simple way to realize such a probe is to employ a transistor of the same family of the one to be characterized or, better, a transistor having a smaller gate area. In Fig. 4 the schematic of our implemented probe is shown. It consists of a JFET, $Q_P$, in a common drain configuration, which has the gate to source capacitance dynamically nulled by the bootstrapping action. To characterize the probe a resistor, $R_{TE}$, is connected very close to the JFET input from one side. The other side of $R_{TE}$ is connected to a step function generator, $V_{TEST}$. In this way the rise time of the output signal is affected by the capacitance, $C_P$, present at the input node, $C_P \approx C_{PA} + C_{GD}$. If the setup is well designed the rise time, $t_R$, of the output signal is dominated by the input pole, given by the product of $R_{TE}$ and $C_P$, resulting in $t_R = 2.2R_{TE}C_P$. If the resistance value is of the order of 1 MΩ (selected with negligible shunting parasitic capacitance), even a capacitance of 1 pF gives about 2.2 μs of rise time, an interval of time very easily measured with conventional instruments. It must be remarked that a sinusoidal swept can be used instead of the voltage step as test signal, which may allow one to obtain even more accurate results.

Once the capacitance of the probe has been measured, the probe is calibrated and it is possible to characterize the input capacitance of any transistor with the connection to the probe input indicated in Fig. 5. The Device Under Test (DUT), the transistor $Q_{DUT}$, is biased in a very simple way. The resistance $R_{SS}$ and the negative supply voltage $V_{SS}$ allows selection of the bias current for $Q_{DUT}$, while the source voltage results self-biased by $R_{SS}$. This is the simplest way to bias a transistor, which does not make use of an additional amplifier for the realization of a DC feedback loop that sets the bias point, which may add instabilities. The drain voltage can be selected with the adjustable positive supply voltage $V_{DS}$. In this way the bias point of the DUT can be made equal to that foreseen in the actual application. For the arrangement shown it results that for both transistors $Q_P$ and $Q_{DUT}$ the gate potential is close to ground at DC through $R_{TE}$ and $V_{TEST}$. In this way the operating voltage for $Q_P$ is unchanged when $Q_{DUT}$ is connected to its input, and the calibration of the probe is not deteriorated.

If now $V_{TEST}$ applies a step voltage to $R_{TE}$ the resulted output at the source of $Q_P$, or of the amplifier $A$, will have this time the rise time...
contributed also by the presence of the input capacitances of \( Q_{DUT} \). The subtraction from the new measured rise time the one obtained from the calibration allows a precise determination of the input capacitance of the DUT. Two kinds of measurements can be made. If the switch SW of Fig. 5 is in the open state \( Q_{DUT} \) is in the common drain configuration and its input capacitance \( C_{GS}, C_{GSD} \) in Fig. 5, is bootstrapped. Since the signal present at the source is \( \gamma \) times that of the gate, with \( \gamma \) close to one, the dynamic effect of \( C_{GS} \) is attenuated to \( (\gamma - 1)C_{GS} \approx 0 \). As such, in this case we measure only the transfer reverse capacitance \( C_{GD}, C_{GD} \) in Fig. 5. If now SW is closed the large capacitance \( C_{SS} \) forces an AC virtual ground at the source of \( Q_{DUT} \), consequently, \( C_{GS} \) now shows its full dynamic effect. The measurement will furnish in this case \( C_J = C_{GD} + C_{GS} \). The extraction of \( C_{GS} \) is possible from the two measurements. The precision in the discrimination between the two capacitances depends on how much \( \gamma \) is close to unity. This can be obtained using a current generator instead of \( R_{SS} \). For this purpose we suggest the configuration in Fig. 6. The operational amplifier \( A_1 \) is fed back to have a voltage gain of two. The current that flows in the resistor \( R_{GSS} \) equals \( (V_G - V_GS)/R_{GSS} \), where \( V_G \) is the gate input voltage and \( V_GS \) is the gate to source voltage of \( Q_{DUT} \). If \( R_{GSS} = R_{SS} \) the balance of the currents at the source node of \( Q_{DUT} \) implies that the drain current of \( Q_{DUT} \) equals \( |V_{SSL}| / R_{SS} \) irrespectively from the input voltage \( V_G \) and the gate to source voltage \( V_GS \). This proves the constancy of \( V_GS \) and that the source voltage \( V_S \) equals the input voltage \( V_G \).

The experimental results obtained have been very good and accurate. In Table 1 the comparison between the measured capacitances at 300 k and at the operating condition of 1 V of \( V_{DS} \) and 1 mA of \( I_{DS} \) are compared with those present in the data sheet for some JFET devices of the Moxtek process. Data sheet did not report the measurement condition for the JFET. It can be seen that the obtained results have been quite different in most cases.

The Moxtek process is especially designed to operate at a low temperature. Data have then been taken also at the optimum temperature of about

Table 1
Comparison between the datasheet and the measured input capacitances for some JFET transistors of the Moxtek process at room temperature. Measurements conditions have been: \( I_{DS} = 1 \) mA and \( V_{DS} = 1 \) V for every transistor. The datasheet specifications do not include the bias condition of the tests

<table>
<thead>
<tr>
<th>JFET</th>
<th>( C_J ) (Datash.) (pF)</th>
<th>( C_{GD} ) (Datash.) (pF)</th>
<th>( C_J ) (Mea.) (pF)</th>
<th>( C_{GD} ) (Mea.) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MX11CA (Moxtek)</td>
<td>1.4</td>
<td>n/a</td>
<td>2.08</td>
<td>0.98</td>
</tr>
<tr>
<td>MX11CD (Moxtek)</td>
<td>7</td>
<td>n/a</td>
<td>4.62</td>
<td>2.59</td>
</tr>
<tr>
<td>MX16 dual gate, gate shorted (Moxtek)</td>
<td>n/a</td>
<td>n/a</td>
<td>76.3</td>
<td>34.6</td>
</tr>
<tr>
<td>MX16 dual gate, ( V_G2 = -0.5 ) V (Moxtek)</td>
<td>5</td>
<td>n/a</td>
<td>4.93</td>
<td>3.74</td>
</tr>
<tr>
<td>MX16C dual gate, gate shorted (Moxtek)</td>
<td>n/a</td>
<td>n/a</td>
<td>43.9</td>
<td>24.6</td>
</tr>
<tr>
<td>MX16C dual gate, ( V_G2 = -0.5 ) V (Moxtek)</td>
<td>n/a</td>
<td>n/a</td>
<td>4.43</td>
<td>3.27</td>
</tr>
<tr>
<td>MX16RC dual gate, gate shorted (Moxtek)</td>
<td>n/a</td>
<td>n/a</td>
<td>43.4</td>
<td>19.6</td>
</tr>
<tr>
<td>MX16RC dual gate, ( V_G2 = -0.5 ) V (Moxtek)</td>
<td>3</td>
<td>n/a</td>
<td>4.11</td>
<td>2.87</td>
</tr>
<tr>
<td>MX170LD (Moxtek)</td>
<td>12</td>
<td>n/a</td>
<td>21.7</td>
<td>12.3</td>
</tr>
<tr>
<td>MX17 (Moxtek) ( V_{DS} = 1 ) V</td>
<td>12</td>
<td>n/a</td>
<td>22.0</td>
<td>12.2</td>
</tr>
<tr>
<td>MX17 (Moxtek) ( V_{DS} = 3 ) V</td>
<td>n/a</td>
<td>n/a</td>
<td>20.7</td>
<td>10.3</td>
</tr>
<tr>
<td>MX17 (Moxtek) ( V_{DS} = 5 ) V</td>
<td>n/a</td>
<td>n/a</td>
<td>19.7</td>
<td>9.5</td>
</tr>
</tbody>
</table>
120 K for the same JFET characterized at room temperature. Results are shown in Table 2. Finally in Table 3 some other commercial devices have been measured at room temperature and compared with the specification of the datasheet.

For the measured JFETs the operating condition has been chosen for obtaining low power dissipation, low noise and small leakage input current. Datasheets indicate measurement conditions and capacitance values that are quite far from those measured. A clear indication of the need to characterize the input capacitance of JFETs is then proven. It must be remarked at this point an interesting observation which regards the calibration of the probe. The probe and the DUT must be put inside a shield to avoid electromagnetic interference. As said above the probe calibration consists in measuring the input capacitance of the probe itself when the DUT is not connected. We have observed the presence of an inaccuracy if only this procedure is adopted. In fact in this case the parasitic effect that the metallic shield adds to the DUT is not taken into account. To account for this it needs to put the DUT in the measuring position and connect only its gate electrode to the probe input, and then proceed in making the calibration. In this way the parasitic capacitance of the DUT towards the shield is taken into account as well. For our setup, designed to fit the input of a nitrogen liquid dewar, the minimal distance between the shield and the DUT is less than 0.3 cm, resulting in a capacitance of about 0.4 pF, not negligible for the smaller devices measured.

<table>
<thead>
<tr>
<th>JFET</th>
<th>Temp.(K)</th>
<th>$C_J$ (Mea.) (pF)</th>
<th>$C_{GD}$ (Mea.) (pF)</th>
<th>$C_J$ room (Mea.) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MX11CA</td>
<td>127</td>
<td>2.23</td>
<td>1.04</td>
<td>2.08</td>
</tr>
<tr>
<td>MX11CD $V_{DS}=3$V</td>
<td>128</td>
<td>6.51</td>
<td>3.07</td>
<td>4.62</td>
</tr>
<tr>
<td>MX16RC dual gate, $V_{GS}=-0.5$V</td>
<td>126</td>
<td>3.75</td>
<td>2.46</td>
<td>4.11</td>
</tr>
<tr>
<td>MX16RC dual gate, gates shorted</td>
<td>122</td>
<td>42.1</td>
<td>19.2</td>
<td>19.6</td>
</tr>
<tr>
<td>MX17OLD</td>
<td>129</td>
<td>21.8</td>
<td>11.8</td>
<td>21.7</td>
</tr>
<tr>
<td>MX17</td>
<td>130</td>
<td>20.8</td>
<td>12.3</td>
<td>22.0</td>
</tr>
</tbody>
</table>

**Table 3**
Characterization at room temperature of some commercial JFET. Measurements conditions have been: $I_{DS}=1$ mA and $V_{DS}=1$ V for every transistor

<table>
<thead>
<tr>
<th>JFET</th>
<th>$V_{DS}$ (V)</th>
<th>$V_{GS}$ (V)</th>
<th>$I_{DS}$ (mA)</th>
<th>$C_J$ (Datash.) (pF)</th>
<th>$C_{GD}$ (Datash.) (pF)</th>
<th>$C_J$ (Mea.)</th>
<th>$C_{GD}$ (Mea.) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IFN146 (Interfet)</td>
<td>10</td>
<td>0</td>
<td>$I_{DSS}$</td>
<td>75</td>
<td>30.5</td>
<td>12.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>$&lt;V_{PINCH}$</td>
<td>0</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SNJ903L43 (Interfet)</td>
<td>0</td>
<td>−10</td>
<td>0</td>
<td>50</td>
<td>84.9</td>
<td>42.8</td>
<td></td>
</tr>
<tr>
<td>IFI40 (Interfet)</td>
<td>15</td>
<td>0</td>
<td>$I_{DSS}$</td>
<td>3</td>
<td>2.63</td>
<td>1.13</td>
<td></td>
</tr>
<tr>
<td>SNJ3600L10 (Interfet)</td>
<td>10</td>
<td>0</td>
<td>$I_{DSS}$</td>
<td>650</td>
<td>481</td>
<td>203</td>
<td></td>
</tr>
<tr>
<td>2SK146 (Toshiba)</td>
<td>10</td>
<td>0</td>
<td>$I_{DSS}$</td>
<td>75</td>
<td>65.5</td>
<td>27.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>−10</td>
<td>0</td>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2N5459 (Fairchild)</td>
<td>15</td>
<td>0</td>
<td>$I_{DSS}$</td>
<td>4.5</td>
<td>4.92 $V_{DS}=1$ V</td>
<td>2.91 $V_{DS}=1$ V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.65 $V_{DS}=2$ V</td>
<td>2.17 $V_{DS}=2$ V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4.49 $V_{DS}=3$ V</td>
<td>1.90 $V_{DS}=3$ V</td>
<td></td>
</tr>
<tr>
<td>2N4416 (Siliconix)</td>
<td>15</td>
<td>0</td>
<td>$I_{DSS}$</td>
<td>4</td>
<td>4.23 $V_{DS}=1$ V</td>
<td>2.01 $V_{DS}=1$ V</td>
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</tr>
<tr>
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<td>4.02 $V_{DS}=2$ V</td>
<td>1.64 $V_{DS}=2$ V</td>
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</tr>
<tr>
<td></td>
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<td></td>
<td>3.91 $V_{DS}=3$ V</td>
<td>1.43 $V_{DS}=3$ V</td>
<td></td>
</tr>
</tbody>
</table>
4. Input current characterization

The proposed method of measurement is suitable also for the accurate characterization of the input current, \( I_G \), of transistors. The setup in Fig. 5 is slightly modified with the addition of a relay with two contacts, shown in Fig. 7. If the relay \( RE_A \) is closed, and \( RE_B \) is open, it is possible to measure the total capacitance \( C_{TOT} \approx C_{CH} + C_{DG} + C_{STRAY} \) present at the input of \( Q_{DUT} \), with the method described in the previous section. If \( RE_A \) is now opened, and \( RE_B \) is closed, the input current of \( Q_{DUT} \) can charge, linearly with time, the measured input capacitance. The voltage present at the gate is expected to be

\[
V_G = \frac{Q_F}{C_{TOT}} + \frac{I_G}{C_{TOT}} t. \tag{15}
\]

In the above equation any possible dissipative effects have been neglected, as will be evident in the following, and \( Q_F \) is the charge injected, by friction at the opening instant, by the relays. The slope, with respect to time, of the resulting wave is proportional to the current itself and inversely proportional to the input capacitance.

This method of characterization is known, but usually since the input capacitance of the DUT is not measured, a selected capacitance, \( C_{CH} \) in Fig. 10, much larger than the expected input capacitance is added to the input to minimize errors, that prevent high sensitivity in the measurement. Since with the present setup it is possible to measure the input capacitance, whatever it is, we can obtain very good precision and even maximum sensitivity when it is put to \( C_{CH} = 0 \).

The relay \( RE \) with the two contacts, \( RE_A \) and \( RE_B \), must be put as close as possible to the transistor input. As described above, when in the current characterization condition \( RE_A \) is open and \( RE_B \) is shorted to ground: the input current can charge the input capacitance and the input link can not inject disturbances on this very high impedance node. This arrangement avoids addition of stray capacitance and error in the measurement given by the connecting wires. This is particularly true when the device is cold and this length it is not negligible.

The input current of the JFET MX11CD by Moxtek was measured at a temperature of about 115 K. As can be extracted from Table 2, the MX11CD has a transfer reverse capacitance of about 3 pF at low temperature. In the setup for the input current characterization the total capacitance resulted in about 7 pF, including stray and the contribution coming from the relay in the open state. The input current of this transistor resulted to be 3 pA at room temperature, when \( V_{DS} \) is 4 V and \( I_{DS} = 1 \) mA. Since \( I_G \) is expected to decrease exponentially with temperature, we expect it to vanish at 115 K. This was what we actually obtained for the drain to source voltage ranging from 1 to 2.5 V. \( I_G \) was permitted to charge the input capacitance for one day, with \( V_{DS} \) equal to 2 V. In Fig. 8 the result is shown. After the charge injection due to the opening of the relays, Eq. (15), which determined a voltage change of about \(-0.25 \) V, the measurement of the source potential has been made every 10 s with a 6.5 digit multi-

![Fig. 7. Measurement setup for input current characterization of transistor \( Q_{DUT} \).](image_url)

![Fig. 8. Source voltage for the JFET MX11CD when the input current \( I_G \) loads the input capacitance and \( V_{DS} = 2 \) V at the start of measuring.](image_url)
plexed multimeter, Keithley 2700. As can be seen after 24 h the source voltage was not yet recovered, showing a linear increase with time at a rate of 2.3 mV/h, or 0.65 μV/s. If we assume the parasitic shunting impedance to be very large, due to an accurate circuit layout implementation, the result corresponds to about $4.6 \times 10^{-18}$ A of gate current.

We changed the value of $V_{DS}$ to observe an unexpected effect. As can be seen in the plot of Fig. 9, where $V_{DS}$ is 4 V at the instant of start of the measurement, the source voltage is not linear with time. The correct explanation of the process is the feedback mechanism which is presented in the setup of Fig. 7. The gate current is strongly dependent on the drain to gate voltage, $V_{DG}$, at large values. As the gate voltage increases, $V_{DG}$ decreases and $I_G$ decreases as well. This effect stops when $I_G$ vanishes, or when $V_{DS}$ is less than about 2.5 V, hence the source voltage remains constant hereon. This hypothesis can be proved if $V_{DG}$ is forced to remain constant during the measurement. With this aim the setup was modified as shown in Fig. 10. The unity gain buffer $Q_{BOT}$ and the source voltage $V_{BOT}$ force $V_{DG}$ to remain constant, irrespective of the gate voltage. The results of the measurements were totally different for this case, showing the expected linear dependence up to the positive supply voltage. With the new setup of Fig. 10 when $V_{DS}$ is 4 V the resulting behavior is shown in Fig. 11. From the slope of the linear part it results in a current $I_G$ of about 85 fA. For this case the input capacitance was measured again, resulting in about 4 pF ($C_{CH} = 0$), to account for the fact that a new bootstrapping effect was introduced between the gate and the drain, due to $Q_{BOT}$ and $V_{BOT}$, which increased the sensitivity further. Measurements were made from 2 to 5 V of $V_{DS}$.

Fig. 12 shows the semi-log plot of the gate current versus $V_{DG}$. We can see that the dependence of $I_G$ with $V_{DG}$ is exponential and that under 2 V of $V_{DS}$ $I_G$ is expected to be totally negligible, $10^{-20}$ A and less.

The same set of measurements has been made with the JFET SN903L by Interfet. In this case the input capacitance of the setup of Fig. 10 resulted in 10 pF. Also for this case $I_G$ has shown the same behavior with respect to $V_{DG}$. Only the value of $V_{DS}$ at which the current started to increase was

**Fig. 9.** Source voltage for the JFET MX11CD when the input current $I_G$ loads the input capacitance and $V_{DS} = 4$ V at the start of measuring.

**Fig. 10.** Input current measurement setup with $V_{DS}$ bootstrapped by $Q_{BOT}$ and $V_{BOT}$.

**Fig. 11.** Source voltage for the JFET MX11CD when the input current $I_G$ loads the input capacitance and $V_{DS}, 4$ V, is forced to a constant during the measurement.
larger since $V_{GS}$ is smaller for this JFET for the same working condition. In Figs. 13 and 14 the source voltage is shown, when $I_{DS} = 1$ mA, for the two cases $V_{DS}$ of 3 and 4 V, respectively. $I_G$ resulted in $5.64 \times 10^{-18}$ A at $V_{DS} = 3$ V and $2.34 \times 10^{-15}$ A at $V_{DS} = 4$ V. Finally, Fig. 15 shows the dependence of the gate current $I_G$ with respect to $V_{DG}$. The exponential dependence of the gate current on $V_{DG}$ also for this case is evident. It can be concluded that JFET must be operated at moderately small, say less than 2 V, drain to source voltages to minimize the gate current at low temperature.

5. Conclusions

A very simple method to measure the input capacitance of transistors has been developed. It allows to discriminate between the input capacitance and the transfer reverse capacitance. The very simple and accurate calibration procedure makes it possible to characterize transistors when operated at cryogenic temperatures, despite the link length.

With this method the input current of transistors can be measured easily, both at room and cryogenic temperatures, with a sensitivity as low as $10^{-18}$ A. It was proved that at cryogenic temperatures the leakage current depends exponentially with the drain to gate voltage and assumes very
small values at moderately small drain to source voltages, 2 V or less.

Acknowledgements

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References