CLARO-CMOS, an ASIC for single photon counting with Ma-PMTs, MCPs and SiPMs

This article has been downloaded from IOPscience. Please scroll down to see the full text article.
2013 JINST 8 C01029
(http://iopscience.iop.org/1748-0221/8/01/C01029)

View the table of contents for this issue, or go to the journal homepage for more

Download details:
IP Address: 149.132.2.36
The article was downloaded on 18/01/2013 at 11:23

Please note that terms and conditions apply.
CLARO-CMOS, an ASIC for single photon counting with Ma-PMTs, MCPs and SiPMs

P. Carniti, G. Cibinetto, A. Cotta Ramusino, A. Giachero, C. Gotti, M. Maino, R. Malaguti and G. Pessina

a INFN, Sezione di Milano Bicocca, Piazza della Scienza 3, 20126, Milano, Italy
b Dipartimento di Fisica G. Occhialini, Università degli Studi di Milano Bicocca, Piazza della Scienza 3, 20126, Milano, Italy
c INFN, Sezione di Ferrara, Via Saragat, 1, 44122, Ferrara, Italy
d Dipartimento di Fisica, Università degli Studi di Ferrara, Via Saragat, 1, 44122, Ferrara, Italy
e Dipartimento di Elettronica e Telecomunicazioni, Università degli Studi di Firenze, via S. Marta 3, 50139, Firenze, Italy

E-mail: claudio.gotti@mib.infn.it

ABSTRACT: An ASIC named CLARO-CMOS was designed for fast photon counting with MaPMTs, MCPs and SiPMs. The prototype was realized in a .35 µm CMOS technology and has four channels, each with a fast amplifier and a discriminator. The main features of the design are the high speed of operation and the low power dissipation, below 1 mW per channel. This paper focuses on the use of the CLARO for SiPM readout. The ASIC was tested with several SiPMs of various sizes, connected to the input of the chip both directly and through a coaxial cable about one meter long. In the latter case the ASIC is still fully functional although the speed of response is affected by the cable capacitance. The threshold could be set just above the single photoelectron level, and with $1 \times 1 \text{ mm}^2$ SiPMs the discrete photoelectron peaks could be well resolved.

KEYWORDS: Front-end electronics for detector readout; Analogue electronic circuits; Photon detectors for UV, visible and IR photons (solid-state); VLSI circuits

1 Corresponding author.
1 Introduction

Several applications in the field of particle physics require detectors capable of counting pulses of single or a few photons at high rates. These include detectors based on Cherenkov light for particle identification, and detectors based on scintillators for tracking and calorimetric applications. The photosensitive devices to be used in such applications can be vacuum-based photodetectors such as multi-anode photomultipliers (MaPMTs) and microchannel plates (MCPs). Modern MaPMTs offer a negligible dark count rate, in the range of a few Hz per pixel, and are thus the preferred choice when single photon detection with low noise is of interest. MCPs on the other side offer a superior time resolution, down to tens of picoseconds, allowing precise TOF measurements. The gain of these detectors is of about $10^5$ to $10^7$ and the pixel capacitance is small, of the order of one picofarad. Whenever more photons are to be detected, an alternative to vacuum-based photomultipliers are silicon photomultipliers (SiPMs), which despite the larger dark count rate are gaining wide diffusion thanks to their low cost and ease of use. The gain of these detectors is still around $10^6$ but the capacitance is larger, being in the range of 10 pF per square millimeter of active area.

The CLARO-CMOS is the first prototype of a preamplifier and discriminator circuit designed for pixellated photodetectors. The prototype has four independent channels, each with its own discriminated (binary) output. In this prototype, two of the four channels have a buffered analog output where it is possible to readout the shaped analog signals. The design of the ASIC was optimized for MaPMTs. The prototype was deeply characterized at the test bench, and the results were presented in [1]. With a source capacitance of a few picofarad a noise of about 6 ke$^{-}$ was measured at the analog output. The pulses are fast, allowing up to a 10 MHz event rate without dead time. The discriminator triggers the pulses with a delay below 5 ns. An outstanding timing resolution was measured with pulser signals on the test bench, obtaining a jitter down to 10 ps RMS. The results can be found in [1]. The power consumption of the prototype is very low, less than 1 mW per channel in idle, and less than 2 mW per channel with an event rate of 10 MHz. Preliminary measurements of the CLARO-CMOS coupled to a R11265 MaPMT are promising, but not yet ready for publication. Also there are plans to test the time resolution of the ASIC coupled to a MCP photodetector, but no results are yet available. When SiPMs are used, the larger capacitance at the input impacts on the speed and noise of the circuit. Even if the design was not
Figure 1. Block schematic of a CLARO-CMOS channel.

optimized for this application, good results could be obtained by coupling the CLARO-CMOS to a SiPM, as shown in this paper.

2 The design of the CLARO-CMOS

A block schematic of a CLARO-CMOS channel is shown in figure 1. The input block is a fast charge sensitive preamplifier with a low input impedance up to high frequency. Details on the design at the transistor level can be found in [1]. The gain of the preamplifier can be adjusted with three control bits. With a negligible capacitive load at the input, the signal at the output of the preamplifier is very fast, with a leading edge of the order of one nanosecond, unless limited by the charge collection time of the detector. With a larger capacitance at the input the leading edge becomes longer of about 100 ps per picofarad of input capacitance, as discussed in [1].

The output of the preamplifier is connected to the inverting input of the discriminator (a voltage comparator), whose non-inverting input is held at a constant voltage generated by the integrated 5 bit DAC. The transistor level schematic of the discriminator can be found in [1]. The voltage of the DAC sets the threshold for the discriminator. Its output gives the fast binary information whether the signal exceeds threshold, and can be used as a trigger for that channel. The CLARO-CMOS is designed to be operated with a 2.5 V supply voltage. The power consumption of the preamplifier, DAC and discriminator blocks is below 1 mW per channel at DC, and increases for large trigger rates, being still below 2 mW for an input signal rate of 10 MHz. The output of the preamplifier is also buffered to the output of the ASIC. The analog buffer is biased with an external resistor, and its power consumption can be tuned to meet the optimal tradeoff between readout speed and dissipated power. With a power consumption in the buffer of about 1 mW and a capacitive load at the output of about 10 pF, the leading edge of the output signal is about 10 ns. This is the case for the measurements presented in the following section.
Figure 2. A picture of the CLARO-CMOS test board with a SiPM in TO-18 package connected to one input. The CLARO-CMOS is enclosed in a QFN48 package, which can be seen at the center of the test board.

Figure 3. Signals at the analog output of a CLARO-CMOS channel with a $1 \times 1 \text{ mm}^2$ SiPM directly connected to the input of the ASIC. The upper signal is taken at the binary output, the lower signal is taken at the analog output. This is a two photoelectron signal taken just above threshold.

3 Measurements with SiPMs

Figure 2 shows a picture of the CLARO-CMOS test board with a SiPM in TO-18 package directly connected to the input. The model used for the tests is a SensL MicroSL-10050-X18 with an area of $1 \times 1 \text{ mm}^2$. The capacitance of this device in operating conditions is close to 10 pF. On the test board the CLARO-CMOS in a QFN48 package can be seen at the center. The signals from the CLARO-CMOS are buffered with fast current feedback operational amplifiers which drive 50 Ω terminated lines to the oscilloscope, a Rohde&Schwartz RTO 1044.
Figure 4. Signals at the analog output of a CLARO-CMOS channel with a $1 \times 1 \text{mm}^2$ SiPM directly connected to the input of the ASIC. The amplitude histogram is shown on the left side of the oscilloscope screen.

The SiPM was biased with 29.0 V and was illuminated by a pulsed LED. The voltage to the LED was adjusted by hand to obtain signals of a few photoelectrons from the SiPM. The threshold of the discriminator of the CLARO was set at two photoelectrons to reject the large number of dark single photoelectron pulses from the SiPM. The oscilloscope was triggered on the binary output of the CLARO-CMOS. Figure 3 shows the oscilloscope screen when a two photoelectron event just above threshold was triggered. The rise time of the binary signal is 2.7 ns, the fall time about 8 ns. The binary pulse width is close to 30 ns. The analog signal has a leading negative edge of about 10 ns, and a trailing edge of about 50 ns. As already mentioned, the speed of the analog signal is limited by the analog output buffer. The analog signal which feeds the input of the discriminator is faster, and this is reflected in figure 3, where the output of the discriminator can be seen to return to the baseline before the analog signal.

Figure 4 shows many analog signals acquired in the same conditions. The capability of resolving single photoelectrons can be appreciated with the threshold set to two photoelectrons. The mean pulse from the LED can be seen to be centered at about 6.5 photoelectrons. The amplitude spectrum was also plotted on the left on the oscilloscope, showing a separation between photoelectron peaks of about one FWHM.

Figure 5 shows the same measurement, except for the fact that the SiPM was connected to the input through a Environflex EF178 coaxial cable with a capacitance of 95 pF/m. The length of the cable was 120 cm. The total capacitance at the input contributed by the SiPM and the cable is thus close to 120 pF. As can be clearly seen in the figure, the analog signals are slower, as expected from the larger capacitance at the input. The increase in series noise expected from the larger input capacitance is mitigated by the bandwidth reduction. The signals corresponding to different numbers of photoelectrons are still well resolved, with a separation between peaks close to one FWHM.

Similar measurements were also performed with other SiPMs, listed in table 1. With $3 \times 3 \text{mm}^2$ devices the noise is larger due to the larger capacitance. Moreover since the dark count rate is close
**Figure 5.** Signals at the analog output of a CLARO-CMOS channel with a $1 \times 1 \text{mm}^2$ SiPM connected to the input of the ASIC with a coaxial cable 120 cm long. The amplitude histogram is shown on the left side of the oscilloscope screen.

**Table 1.** List of SiPM and MPPC devices tested with the CLARO-CMOS.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Size</th>
<th>Pitch</th>
<th>Device name</th>
</tr>
</thead>
<tbody>
<tr>
<td>AdvanSid</td>
<td>$1 \times 1 \text{mm}^2$</td>
<td>50 µm</td>
<td>ASD-SiPM1S-M-50</td>
</tr>
<tr>
<td></td>
<td>$1 \times 1 \text{mm}^2$</td>
<td>100 µm</td>
<td>ASD-SiPM1S-M-100</td>
</tr>
<tr>
<td>Hamamatsu</td>
<td>$1 \times 1 \text{mm}^2$</td>
<td>50 µm</td>
<td>S10362-11-050U</td>
</tr>
<tr>
<td></td>
<td>$1 \times 1 \text{mm}^2$</td>
<td>100 µm</td>
<td>S10362-11-100U</td>
</tr>
<tr>
<td></td>
<td>$1 \times 1 \text{mm}^2$</td>
<td>50 µm</td>
<td>S10362-11-050C</td>
</tr>
<tr>
<td></td>
<td>$3 \times 3 \text{mm}^2$</td>
<td>50 µm</td>
<td>S10931-050P</td>
</tr>
<tr>
<td>SensL</td>
<td>$1 \times 1 \text{mm}^2$</td>
<td>50 µm</td>
<td>MicroSL-10050-X18</td>
</tr>
<tr>
<td></td>
<td>$1 \times 1 \text{mm}^2$</td>
<td>100 µm</td>
<td>MicroSL-10100-X18</td>
</tr>
</tbody>
</table>

to $10^7$ counts per second pile-up from the dark single photoelectron events occurs, and the discrete photoelectron peaks cannot be clearly separated. Anyway the threshold in this case can still be set at the level of a few photoelectrons. In the case of Hamamatsu MPPC devices, where holes are meant to be collected at the readout electrode, the $n$ substrate was connected to the input of the CLARO-CMOS in order to get negative signals at the input. For specific use with such devices a dedicated version of the ASIC could be designed, keeping the same topology and changing N-MOS transistors with P-MOS and vice versa, and exchanging the discriminator inputs.

**4 Conclusions**

The CLARO-CMOS, a prototype ASIC for fast photon counting was presented. The design offers a high speed of operation, being able to sustain event rates up to 10 MHz, with a very low power
dissipation, in the range of 1 mW. The ASIC was tested with several SiPM devices from different manufacturers. With a 1 mm$^2$ SiPM, both directly connected to the input and through a 120 cm coaxial cable, the signal amplitudes corresponding to the discrete few photoelectrons signals could be well resolved.

References