A Low Dc Drift Read-Out System For A Large Mass Bolometric Detector

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Abstract

We present a read-out system for large mass bolometric detectors. It consists of a differential voltage-sensitive preamplifier having very low series and parallel noise, thanks to the use of a pair of selected silicon JFET at the input. Very good electrical characteristics were obtained. DC power supply rejection ratio, thermal drift of input offset voltage and input leakage current are minimized by using novel circuit solutions. Parallel noise behavior was also investigated using a new measurement method which is sensitive to the shot noise generated by very small currents (tens of fA).

I. INTRODUCTION

A large mass bolometric detector consists of two parts. 1) An energy absorbing crystal cooled to very low temperatures, (~10 to 100 mK) to get minimal heat capacity. In this way an energetic particle which impinges onto the crystal, releasing all or part of its energy, is able to increase the temperature by a measurable amount, inversely proportional to the heat capacity itself. 2) A temperature sensor, a thermistor in our case, put in good thermal contact with the crystal, converts the temperature increase into an electrical signal, read-out by a low-noise preamplifier. The thermistor has a static resistive impedance, in the tens of MΩ range. Its dynamic component shows also an inductive effect [1].

During the last few years we have progressively increased the mass of our detectors [2], with the consequent shift of the signal energy spectrum toward lower frequencies, down to a few tens of Hz. The low parasitic capacitance of cold electronics, previously used [3], was no longer required, as now the detector resolution is not affected by large stray capacitances.

These detectors, which can reach in principle a very high energy resolution [4], can be read-out by a fully DC coupled system or, alternatively, they can be AC biased, in which case the slow signal will amplitude-modulate the sinusoidal bias voltage across the thermistor. An AC bias system is presently under study. The DC bias approach, subject of this paper, requires a read-out with low series noise at low frequencies and low parallel noise. This is necessary to process detector signals contained in bandwidth of a few tens of Hz, as those developed on the large resistive impedance of the detector. Energy conversion gain variations are always present, possibly generated by slow thermal drift of the cryogenic system. The read-out system can be sensitive enough to these fluctuations if it has a very low drift.

It can be shown that under the usual working conditions of our large mass bolometers, the parasitic capacitance shunting the thermistor has effects on the energy resolution performance only when it becomes of the order of hundreds of pF [5]. A read-out system with the preamplifier put outside the refrigerator, a few meters away from the detector, could in principle be a practical solution. A possible drawback could come from the microphonic noise due to the vibrations of the connecting link, proportional to the length of the wires. Still this common mode noise can be minimized by adopting a differential configuration for the preamplifier.

In this paper a new Differential Voltage-Sensitive Preamplifier (DVSP) designed for the read-out of an array of 20 TeO₂ bolometers, 330 g each, is described. To obtain both very low parallel and 1/f series noise, a pair of silicon JFETs has been used at the preamplifier input. Although a discrete preamplifier has been realized, very good dynamic and static performances have been obtained, very close to that achievable with good monolithic circuits. This was possible by using non standard circuit configurations.

In the following sections the steps for the development of the complete DVSP will be described. The DVSP drift voltage was minimized by implementing a very large DC Power Supply Rejection Ratio (PSRR), as described in section II, and a very low thermal drift, section III. In particular the low thermal drift was obtained thanks to the use of a new compensation procedure. In section IV the study of the static and noise behavior of the input leakage current is illustrated. Results were used to optimize the bias of the input JFETs. In the same section a new method which allows to measure parallel noise at very low levels is illustrated as well. In section V the complete circuit of the preamplifier is shown and described. Finally section VI describes the temperature stabilization and cooling of the input JFETs of the DVSP, necessary to minimize the input leakage current.

II. PREAMPLIFIER REJECTION TO POWER SUPPLY

We firstly describe the Power Supply Rejection Ratio (PSRR) which at DC must be very high to minimize the baseline fluctuation in the data acquisition system. The DVSP shows a PSRR of about 75 dB. To increase it further we decided to implement a very stable voltage supply based on the BB REF-102 device, a monolithic 10 V reference voltage chip, having 1 ppm/°C drift and 110 dB of PSRR. Its output voltage was buffered to be able to drive a current of about 150 mA, or 5 preamplifiers. By using two such devices and two
buffers, a symmetric ±10 V supply voltage was obtained. To measure the DC PSRR, the supply voltages (±12 V) of the REF102 and buffer system were varied in small steps, at intervals of about 4 min each, obtaining a triangular wave of 2 hs period and 1 V amplitude. LabView software was used to modulate the supply voltages (adding the offset of an HP3314A signal generator to a ±12 V floating voltage source) and to measure both the supply voltage and the preamplifier output with an HP3478A multimeter, whose input was multiplexed by means of two relays.

The supply voltages were varied one at a time. PSRR was determined by finding correlation between the shape of the applied signal and the DVSP output, after the DVSP reached the stabilization (~5 hs). The estimated sensitivity of the measurement chain was about 147 dB. The negative (-12 V) supply PSRR was determined to be 146 dB, while for the positive supply we obtained 137 dB. Figure 1 shows the measurement results. The DVSP voltage gain was 218.

The results obtained were satisfactory. A preamplifier input voltage drift of 0.5 µV/°C was obtained as a typical value. The lowest drift was 0.1 µV/°C. Figure 3 shows the input offset voltage recorded over a few days, showing the long term stability of the system. The room temperature, following the laboratory conditioning system, is also shown. LabView was used to read, every 3 minutes, the DVSP output and a platinum resistive thermometer. The average drift is about 0.5 µV/°C, which becomes 0.7 µV/°C if we consider that during the day doors are continuously opened and closed, (setting sharp changes of room temperature) and people move around. It must be noted that without the correction circuit, the thermal drift of the preamplifier alone was never less than 10-30 µV/°C.

III. THERMAL DRIFT SUPPRESSION

The DVSP offset voltage drift must be as small as possible, to be able to monitor variations in the signal baseline. Small drift is not simple to be realized in general, and in particular when a preamplifier is implemented with discrete components, as in this case. The standard approach would be to look for good thermal matching of the sensitive devices. We have adopted a different approach, based on practical considerations, as described below.

The thermal drift in a limited temperature range has a linear dependence with temperature. This is the case with discrete metal film resistors or base-emitter or gate-source voltages of transistors. Let's assume, for the moment, that a possible imbalance of the input leakage currents does not generate a measurable offset voltage on the source input impedance. We then expect that if a mismatch between components inside the circuit is present, the preamplifier output voltage changes linearly with temperature.

Instead of looking for the source of the mismatch, the adopted solution tries simply to compensate for the existent drift. For that purpose a voltage or current source Proportional To the Absolute Temperature (PTAT) must be realized. The principle of operation of the adopted solution is illustrated in figure 2. A 2 µA/°C current generator, whose circuit implementation is described in detail in section V, was realized. Regulation of trimmer T2 permits to add an amount of thermal current, with a polarity opposed to the unwanted present drift, in proper differential nodes of the preamplifier circuit.

![Figure 2: Schematic diagram of the PTAT current generator.](image_url)

IV. INPUT LEAKAGE CURRENT STUDY

The input leakage current may create two important effects: parallel noise and offset voltage across the source input impedance (if there is an imbalance between the two bias currents). Leakage current was studied in two steps. Firstly we looked for a dependence on the reverse drain to gate and source to gate voltages, to optimize the bias of the input JFETs. Secondly, a measurement of the parallel noise as a function of the static measured leakage current was made, to investigate for effects other than the expected pure white shot noise. The input leakage current was measured using a HP3314A signal generator, whose output was added to a ±12 V floating voltage source. The leakage current was determined by finding the minimum value of the output noise, with a HP3478A multimeter. The leakage current was found to be 0.5 nA for a ±12 V supply voltage. The leakage current was found to be inversely proportional to the supply voltage, with a slope of approximately 0.1 nA/V. The leakage current was then measured over a period of 24 hs, using a HP3478A multimeter. The leakage current was found to be stable, with a maximum variation of 10% over the period. The leakage current was then measured over a period of 30 days, using a HP3478A multimeter. The leakage current was found to be stable, with a maximum variation of 5% over the period.
noise. For both measurements special set-ups were implemented.

A. Static Measurement of the Leakage Current

Input leakage currents ($I_{LE}$) of input JFET transistors are due to the gate-to-channel junction reverse voltage. The dependence of $I_{LE}$ on the junction reverse voltage is expected to follow the law [7]:

$$I_{LE}(T, V_R) = I_S(V_R)\exp\left(-\frac{E_G}{\eta k_B T}\right).$$

In eq.(1) $E_G$ is the silicon energy gap, $k_B$ the Boltzmann constant and $T$ the absolute temperature. $\eta$ is a parameter which is equal to 1 when the dominant current is of diffusion type, 2 when it is of generation-recombination (G-R) type. In the latter case the saturation current $I_S$ will depend on the width of the depletion region which, in turn, depends on the reverse voltage, $V_R$, with a law which is a function of the doping profile. In silicon, at low doping concentration, like those used for the channel of JFETs, the G-R current is dominant and a dependence on the reverse voltage is expected.

We have investigated this dependence in order to optimize the drain to source voltage of the input transistors, Toshiba 2SK146. For the measurements the device was configured as a diode, with the drain and source connected together. A special procedure was implemented to correct for the offset current of the reading circuit. The set-up is shown in figure 4.

To compensate for the input leakage current of the preamplifier, $I_{PRE}$, during the measurement, we added a diode $J_1$, adjusting its reverse voltage $V_{COMP}$ to force $I_{COMP}$ to be equal to $I_{PRE}$, while switch SW is open. The condition $I_{COMP} = I_{PRE}$ is reached when the output voltage is stable. In this way, after closing SW, the output voltage is expected to depend only on $I_{LE}$. The capacitance $C_{INT}$ is then charged with $I_{LE}$. The time interval between two different reference values of the output voltages is inversely proportional to $I_{LE}$.

The current was measured as a function of both reverse voltage and temperature. Temperature was varied in steps of 10 °C, from room temperature to about -20 °C, using a Peltier cell to cool the JFET transistors.

The indication that the current is of G-R type and the presence of a parasitic resistance were taken into account to find the final interpolation functions shown in figure 5. The actual function used for the interpolation was (see also eq.(1)):

$$I_{LE}(T, V_{DG}) = I_S(V_{DG})\exp\left(-\frac{E_G}{\eta k_B T}\right) + \frac{V_{DG}}{R_{PAR}}.$$  

Fits of the data returns $E_G/(\eta k_B) = 6385$ K, in good agreement with the theoretical value.
agreement with the theoretical value of 6667 K, for G-R type current behavior. Measurements accuracy can be seen as well normalizing all data with the leakage current measured at room temperature, to be independent from the reverse voltage. From eq.(2) a new dimensionless function \( \gamma_{LE}(T) \) can be introduced which satisfies:

\[
\gamma_{LE}(T) = \frac{I_{LE}(T, V_{DG}) - \frac{V_{DG}}{R_{PAR}}}{I_{LE}(300K, V_{DG}) - \frac{V_{DG}}{R_{PAR}}} = \exp\left(\frac{-E_G}{\eta K_B T}\right) \tag{3}
\]

As can be seen in figure 8 all the normalized data fits very well with interpolation.

The leakage current for these devices is very low when bias voltage is fixed to be less than 1 V, which is a limiting operating point to get good dynamic characteristics. Moreover, if the temperature of operation is fixed around 0 °C, or less, \( I_{LE} \) is lower than 10 fA, becoming limited at most by a parasitic resistance of 15 TΩ. It must be noted that this resistance generates a parallel noise equivalent to a shot noise generated by a current of only 5 fA.

The same kind of measurements have been done with the devices connected as transistors at the input of the DVSP. No appreciable differences were observed in the dependence of the leakage current with temperature, compared to the diode configuration case.

**B. Input Parallel Noise Measurements**

Studies on parallel noise must be performed to understand whether its origin is pure shot noise of the leakage current (shot noise of G-R origin has Lorentzian components [9]), or if there are contributions also from other sources, like second stage or common mode disturbances.

A classical way to perform this test is to employ a bias resistor of large value to reference the preamplifier input to ground [10], [11]. Due to the low level of shot noise we want to investigate, generated by a current of less than 100 fA, we need at least 1 TΩ resistor, to have a negligible parallel thermal noise. Another approach is to implement a resonant circuit with capacitors and inductors at the preamplifier input, to enhance parallel noise contribution in a tuned, narrow, frequency bandwidth [12]. Both methods are not suitable for the present application. The first one because of the very large value needed for the reference resistor, the second one because it is very difficult to get a low tuned frequency, close to DC, as we need.

The adopted approach was instead very simple and efficient. A non dissipating input load impedance was used (a capacitance). Data was taken at different temperatures, looking for a correlation between measured noise and static current measurements. This way it was possible to separate shot noise effects from other sources of parallel noise, because the former depends exponentially on temperature, while other effects generally don’t, especially if the only cooled device is the JFET itself.

The set-up implemented is an elaboration of a method already adopted for a solid state detector biasing [13], where a reverse biased diode is used to load and compensate for the detector leakage current. For the present case we have used a “diode connected” JFET, similar to the one located at the preamplifier input, to feedback the preamplifier (figure 9). In this way the preamplifier input leakage current, \( I_{LE} \), is forced into the feedback diode \( J_F \), which biases itself in the reverse region, with a voltage close to the drain-to-gate voltage of the preamplifier input JFET, \( J_1 \). From here on, drain-to-gate and drain-to-source voltages are considered equal, because the transistors are operated close to the saturation current \( I_{DSS} \).

The reverse biased junction behaves as a capacitance (\( C_T \)) into which the leakage current is integrated. The noise of \( J_F \) is
the same as that of $J_1$; we expect to measure twice the parallel noise of the input transistor $J_1$. Output noise due only to parallel noise should be:

$$V_O^2 = \left| \frac{\alpha(\omega)}{\omega C_F} \right|^2 2(2qI_{LE});$$

(4)

where $\omega$ is the angular frequency, and $\alpha(\omega)$ is a correction factor which takes into account the fact that the preamplifier is not ideal. Since the feedback capacitance $C_F$ depends on the diode bias condition, its value is not known "a priori". For this reason the actual frequency response is measured by injecting a test signal by means of a capacitance $C_T$ of known value:

$$T_F(\omega) = \frac{\alpha(\omega)}{\omega C_F} \Rightarrow \left| \frac{\alpha(\omega)}{\omega C_F} \right|^2 = \frac{|T_F(\omega)|^2}{\omega C_T};$$

(5)

Both the noise and the frequency response were measured with the help of a dynamic signal analyzer HP3562A. The noise measured at the preamplifier output, using eq.(4), is referred to the input by means of the measured $T_F(\omega)$, given by eq.(5). By dividing also by the $a$ factor $2(2q)$ an equivalent shot noise current is obtained. As an example figure 10 shows the equivalent input shot noise for $V_{DD}$ equal to 1 V, obtained at two different temperatures of operation: room temperature and -23 °C. As it can be seen, the equivalent noise is white in the frequency range considered. Measurements were taken at different temperatures and drain-to-gate voltages (1 V and 3 V).

So far the results obtained include both parallel noise and all the possible contributions to parallel noise coming from second stage and common mode signals. To discriminate between the two effects we looked for a correlation between measured noise and static leakage current. The correlation considered was:

$$I_{LEN} = I_{LE} + I_{LEN}(V_{DD}) + I_{HIST};$$

(6)

where $I_{LEN}$ is the total measured noise current, $I_{LE}$ is the static current measured as shown in section IV.A, $I_{LEN}(V_{DD})$ is a term which takes into account a noise behavior different from pure shot noise and, finally, $I_{HIST}$ is the possible contribution coming from second stage. Results obtained are shown in figure 11. It can be seen that there is a contribution for $I_{LEN}(V_{DD})$, of about 60 fA/$V_{DD}$ as a rough approximation. The cause is not yet understood. It can be excluded that this is related to the intrinsic voltage gain of the input transistors, otherwise the expected effect should be in the opposite sense. The induced, correlated noise coming from the channel [9] cannot justify the observed effect, either. A source of noise, of about 250 fA, independent of leakage current is also present at $V_{DD}$=1 V. This is mainly due to common-mode noise coming from supply voltages, which, in this circumstance, were not the ones adopted and described in section II. If in this non-differential set-up only the shot noise of the input JFET were present, the equivalent input current for the mentioned source of noise would be two times larger (500 fA).

We will investigate further the behavior observed, by setting different drain to gate voltages. We also plan to improve this already extremely sensitive method, trying to realize a true differential parallel noise measurement, by connecting another diode at the second input of the DVSP.

So far it has been proved that when the JFETs are biased with $V_{DD}$ equal to 1 V and operated at a temperature lower than 0 °C, equivalent parallel shot noise has a pedestal of 60 fA, although leakage current becomes negligible. If not operated in true differential way, which is not the case for the present application, a supply voltage effect is observed which may increase the equivalent parallel noise to even 400 fA.

V. DVSP CIRCUIT DIAGRAM - NOISE PERFORMANCE

All the results described in the previous sections, have been taken into consideration for the design of the DVSP. The whole circuit is illustrated in figure 12. Use of a few Operational Amplifiers, OAs, has been adopted to obtain good symmetry. The circuit board is 2.5 X 3 cm²; the input JFET can be mounted on the board, or far away, if cooled.

The pair of input transistors $Q_1$ and $Q_2$ is cascaded by the JFETs-OAs combination realized with transistor $Q_3$ and $Q_6$ and two OAs (3/4 and 4/4 of a quad TL074). The reference
voltage for the cascode combination is the virtual ground present at the middle point of the feedback resistors \( R_5 \) and \( R_6 \), connected at the sources of \( Q_1 \) and \( Q_2 \). In this way the drain to source voltages of \( Q_1 \) and \( Q_2 \) are fixed to 1 V, optimizing input leakage current, independently from the common mode input voltage. The cascode output is converted from differential to single-ended by the low noise OA OP27. The structure is feedback with the resistors \( R_5 \), \( R_6 \) and \( R_7 \), \( R_8 \). The resulting closed-loop voltage gain, given by \((1+R_7)/R_5\), is 218. It must be noted that the circuit has a high input impedance despite the use of only one pair of input transistors. Sink currents of 1 mA each for transistors \( Q_1 \) and \( Q_2 \) are given by the current generator formed with \( Q_4 \), \( R_2 \) and \( 1/4 \) of the TL074.

Final considerations concern the offset adjustment, and the PTAT operation. Since they must generate a common-mode imbalance, great attention was put in their implementation, to avoid negative effects on both dynamic and noise performances. Output offset voltage adjustment is made through a current generator formed by \( Q_6 \), \( R_8 \), one OA \((2/4 \text{ TL074})\) and the trimmer \( T_1 \). \( T_1 \) is connected to the circuit at nodes A and B, which, being of low impedance, avoids possible problems with asymmetry coming from non perfect balance of load impedances. Maximum current is about 250 \( \mu \text{A} \), with which a compensation of \( \pm 22 \text{ mV} \) of input DC differential voltage (i.e. the detector bias) is possible. To generate this low current, a large value resistor \( R_1 \) must be used. This assures enough degeneration for noise and drift of the current generator itself.

The same nodes A and B are used to feed the thermal offset current coming from the PTAT generator, composed by the monolithic reference source voltage LM35, which develops 10 mV/°C, and the two OAs \((1/2 \text{ and } 2/2 \text{ TL072})\). The two OAs convert the voltages at their inputs into two currents, one of each having a thermal drift of 2 \( \mu \text{A/°C} \) derived from the LM35. The resulting output current injected into the trimmer \( T_2 \) is the thermal current indicated in figure 2, plus a small offset current of about 10 to 20 \( \mu \text{A} \). The PTAT is therefore capable to compensate up to 360 \( \mu \text{V/°C} \) at the DVSP input. Non compensated DVSP input drift voltage is of the order of 10 to 30 \( \mu \text{V/°C} \). Since this is about 10\% of the PTAT current, only a small amount of it is needed to compensate the preamplifier drift, minimizing noise effects of the PTAT network.

Preamplifier series noise is shown in figure 13. At a frequency of 0.1 Hz the noise is less than 100 nV/√Hz. It rolls-off following a Lorentzian spectrum, as expected for a device having a single trap in the energy gap. At 1 Hz the noise is less than 30 nV/√Hz, and becomes 5 nV/√Hz at 10 Hz. Integrated noise between 0.1 and 10 Hz is less than 80 nV_{\text{rms}}. With a detector energy conversion gain of about 0.9 mV/MeV, and a bolometer impedance of 520 MΩ, the equivalent energy noise due to the DVSP is 290 eV Full Width Half Maximum (FWHM), with 60 fA of input leakage current at each DVSP input. This result has to be compared

![Figure 12: Complete circuit for the Differential Voltage Sensitive Preamplifier (DVSP).](image-url)
with the actual detector energy resolution of about 3 KeV FWHM [14].

As far as dynamic performances are concerned, the DVSP has a frequency bandwidth limited to a few kHz, and a Common Mode Rejection Ratio of about 85 dB from DC to about 1 kHz. Integral non linearity is 0.05 % for ±6 V output voltage swing, corresponding to ±27.5 mV variations in the differential input.

VI. TEMPERATURE STABILIZATION AND COOLING OF INPUT JFET TRANSISTORS

Input JFETs have a leakage current of about 330 fA at room temperature, which reduces to about 10 fA if the temperature is of the order of 0 °C. We therefore decided to lower the temperature of the JFETs. Since the experiment is located inside a Faraday cage, a DC ‘cooling’ system was realized, to avoid the introduction of line cables inside the cage. A 5.5 W power capability Peltier cell, capable to set a thermal gradient of ±65 °C, was placed on the floor of an hermetic metallic box. Two JFETs and two platinum thermometers were put in good thermal contact with the cell by means of a spring system. The metallic box was thermally connected to a heat sink, having 0.3 °C/W thermal resistance, and it was evacuated with a peristaltic pump, to reduce thermal contact between the Peltier cell and the laboratory environment. The minimum temperature registered by the thermometers in this configuration was -23 °C.

One of the two thermometers was used for stabilizing the temperature at -6 °C. The stabilization circuit is shown in figure 14. It is based on the use of the monolithic instrumentation amplifier BB INA118, able to feature a voltage gain of 10000 with an input offset drift voltage of less than 0.1 μV/°C. A double feedback was realized. The INA118 was made unity gain stable by adding a dominant pole, Rc,1. A driver was connected at the output, able to feed the suitable current to the cell (about 2 A). A capacitor Cf, of very large value, was then added to give to the amplifier a unity gain frequency bandwidth of less than 4 Hz. This configuration guarantees that when the temperature of the cell is regulated, the resulting second feedback loop is stable.

Residual thermal conductance between the devices put on the cell, inside the box, and the laboratory environment was compensated by stabilizing the internal box temperature to a few degrees over room temperature. A heater, a long strip platinum thermometer and a circuit similar to that shown in figure 14 were used for the purpose. In this way the temperature of the devices on the cell reached a stabilization of 40 m°C/°C, while the temperature inside the box varies 100 m°C/°C. This condition was obtained at a temperature of -6.3 °C (see figure 15), where the leakage current is less than 10 fA.

When the input JFETs are cooled and stabilized, together with the box temperature, the DVSP is able to reach a thermal drift of less than 5 μV/°C, if the thermal drift compensation is not used. The result approaches the one shown in section III, if thermal compensation is put into operation.

VII. SUMMARY AND CONCLUSIONS

A Differential Voltage Sensitive Preamplifier (DVSP) capable to fulfill the specifications required to read out signals coming from a bolometric detector of large mass was realized. New circuit solutions and measurement methods have been implemented. Table 1 shows the performances obtained for the DVSP. Input offset voltage thermal drift was very low, despite the use of discrete active devices, thanks to a new circuit design, able to compensate for the preamplifier drift. The use of discrete input JFET transistors permitted to obtain low series noise and input leakage current. Intensive experimental studies have been done on the leakage current
behavior with bias conditions and temperature. Very accurate static measurements of reverse leakage current of these pn junctions were performed using an offset compensation procedure.

The introduction of a new measurement method allowed to measure shot noise down to $3.2 \times 10^{-33} \text{A}^2/\text{Hz}$, corresponding to a current of 10 fA. In this way it was possible to determine that the actual parallel noise was larger than what expected from pure shot noise, and it was proportional to the drain-to-gate voltage ($V_{DG}$) of the input JFETs. At a temperature lower than 0 °C, the leakage current $I_{LE}$ was negligible, but a pedestal of an equivalent shot noise of 60 fA was observed for 1 V of $V_{DG}$. For 3 V of $V_{DG}$ the pedestal increased to 180 fA. The resulting series noise was very low, see table 1.

Input JFETs transistors can be operated both at room temperature and at -6 °C to minimize parallel noise, by using a Peltier cell. A circuit was developed to stabilize the JFETs temperature. Stability was better than 50 m°C/°C, limited by the residual thermal conductance of the JFETs toward the ambient.

VIII. ACKNOWLEDGE

The intensive and invaluable technical support of Maurizio Perego was much appreciated.

IX. REFERENCES


Table 1

<table>
<thead>
<tr>
<th>Differ. Vol. Gain</th>
<th>FSRR (Rej. To Sup.) (dB)</th>
<th>CMRR In. Com. Re. (dB)</th>
<th>Integral non linearity (%)</th>
<th>Input Offset drift voltage $\mu$C</th>
<th>Input Leakage Current (fA)</th>
<th>Eq. Shot noise $2qI_{EQ}$ (fA)</th>
<th>Input series noise (nV/√Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>218 with a few KHz BW</td>
<td>137 ($V_{CC}$)</td>
<td>85</td>
<td>0.5 (±8V Out)</td>
<td>0.05 (±6V Out)</td>
<td>&lt;0.5</td>
<td>330</td>
<td>100 @ 0.1Hz</td>
</tr>
<tr>
<td></td>
<td>146 ($V_{BE}$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>380</td>
<td>26 @ 1Hz</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td>60</td>
<td>5 @ 10Hz</td>
</tr>
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</table>

A voltage of 30°C would be more suitable for the experiment.
