The Production Readiness Review for the distribution boards of the High Voltage at RICH1 and RICH2

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1. The system configuration

In this report we will describe the High Voltage, HV, distribution system for both detectors RICH1 and RICH2, RICHx [1], [2], [3]. Each detector is composed of arrays of Hybrid PhotoDetectors, HPDs, having the front view shown in Figure 1. Any floor is composed of columns. RICH1 has 2 floors and 7 columns with 14 HPDs per column, while RICH2 has 2 floors with 9 columns and 16 HPDs per column. On the back of each column the electronics is housed, organized as shown in Figure 2.

![Figure 1: One floor of RICH2 detector.](image)

The signals that out from the HPD are processed from the L0 board, located closed to it [4]. The LV board provides the voltage supplies for both the L0 board and the silicon pixel array chip on the HPD itself [5]. In addition, the LV board is in communication with the control room. This way the slow controls signals of the L0, LV and HPD can be managed. Moreover, the monitoring of the temperature and supplies voltages allows also obtaining a safe control of this part of the detector system.
The PRR for the HV boards of RICH

Figure 2: The simplified diagram of one column of RICH2 detector.

The High Voltage, HV, boards provide the distribution of the 3 HVs necessary to bias the HPD tubes, see below. The cabling of the HPDs to the HV boards are visible from the top view of the column, Figure 3.

The schematic details of the HPDs are in Figure 4. At the HPD output it is present a pixel chip that maps the photoelectrons in 2D. The photoelectrons are generated in the photocathode, after the quartz window. They are subjected to acceleration, focusing and magnification after the application of 3 HVs across the tube, -20 KV, -19.7 KV and -16.4 KV.

The subject of this document is to provide the description of the distribution system of the HVs to the HPDs of both RICHx.

Figure 3: Top view of the column.
2. The schematic distribution of the High Voltages

From the point of view of the HV distribution, every column of RICHx is considered split in two half-columns. The two half-columns will be fed (in the centre of the column) with two separate -20 KV voltage connections, that will come from the control room, about 100 m far from the detector, Figure 5.

The remaining -19.7 KV and -16.4 KV will be generated from the -20 KV inside the half-column, in a manner described below. Using only one HV to enter any half-column allows improving safe operation with respect to a multi supply solution. This way it can not be verified that one voltage stop completely to work, due to compliance, while any other voltages is still into full operation: there is present a correlation between the 3 lines at all time.

The generation of the 3 HVs inside the half-column is shown in the diagram of Figure 6 (taken from RICH2). Two different types of Printed Circuit Boards, PCBs, have been developed to absolve 3 tasks. The PCB type A can be equipped with a custom voltage divider resistor able to out the 3 HVs starting from the -20 KV. Some filtering capacitance are included that allow to reduce noise. In this Type A board there is also present a protection network that biases 2 HPDs. In addition the 3 HVs are made available to the next board, Simple Board, which is the same kind of board without the voltage divider and the filtering capacitances, but with the protection network that provides the biasing of another pair of HPDs. A third Simple Board will have the same characteristics of the previous board. Finally the last board of the half-column is the Type B board.
**The PRR for the HV boards of RICH**

It provides the biasing of the last pair of HPDs and is equipped with a network that allows the monitoring of the 3 HVs.

As can be seen in **Figure 6** The Simple Boards are either of Type A and Type B. This choice has been adopted for using the same number of boards, saving in production cost.

**Half Column (8 HPDs)**

![HV distribution schematic diagram](image)

*Figure 6: HVs distribution schematic diagram inside the half-column of RICH2.*

### 3. Ground connections of the column.

The main ground connection for the RICH detectors is the one coming from the safety ground (control room). Safety rules require that the metallic frame of the columns have to be connected to this safety ground. The same point of connection is exploited by the jacket of the high voltage cable. The last grounds of the column come from the L0 and LV boards.

To reduce as much as possible the risk of ground loops we have tested with good results the ground scheme of **Figure 7**. The safety ground of the laboratory is connected to the column frame in the centre, between the LV and the HV boards. At the same point it will be connected the shield, jacket, of the high voltage cable connected to the external power supply.

The shields of the HV cables do not fully satisfy the safe condition rules, therefore we recommend to route in parallel to the two HV cables of the column a large cable joint by bolts, to connect the safety ground firmly.

The floating HV power supply will be provided with a device able to limit its common mode voltage with respect to the safety ground.

The last connections needed are the grounds of the L0, LV and HV boards. These connection are necessary to close the path of the photocurrents that flow from the HV photocathode of the HPDs to the pixel chip and to its ground.

All of these connections will concentrate at the centre of the column. Thanks to the fact that the low voltage power supply will be floating, it will be realized a “star” configuration.

To avoid as much as possible ground loops a single ELMB board, biased with a floating power supply, will monitor a half-column, so as to connect its ground to the column one.
4. Circuit description of Board Type A

The schematic diagram of the board Type A is shown in Figure 8. When it is located in the middle of the column Type A board is fully populated. The inputs to the board (left side in the figure) are the -20 KV and GND1 lines. The voltage is applied to the voltage splitter; a custom device [6] (see Appendix A for specifications) designed having the resistor values and ratio as shown in the figure. Some filtering capacitances are put in parallel to the splitter [7]. The outputs of the voltage splitter are the 3 HVs on the right, -20 KV, -19.7 KV and -16.4 KV and GND2. These HVs and GND2 are connected to the next board in the column and also to a pair of HPDs through a protection network consisting in 3 resistors of adequate value [8], see Figure 8.

Further details must be given to explain the presence of the terminals GND1, GND2 and resistor Rsens with which we perform an analog boundary scan. In normal operation GND1 and GND2 are connected together, featuring a low impedance track. When the board has to be tested, just after production, GND2 is left floating, and resistor Rsens is not short circuited. This way it is possible to monitor the leakage current of the board across Rsens for characterization and pass-fail test.

This board is used also as the Simple Board of Figure 6. In that case the voltage splitter and the filtering capacitances are not mounted and at its inputs must be provided the 3 HVs.
5. Circuit description of Board Type B

The board Type B is in Figure 9. It has at its inputs the 3 HVs and GND1 (on the right in the figure). These lines are out to the next board in the column, if present, and are distributed to a pair of HPDs through the protection resistors. This board has additional outputs that allow monitoring the HVs. This task is performed by means of a partition between the 5 GΩ resistors and Zmo’s, resistors of a few MΩ value. Zmo is actually a parallel combination of a resistor, a capacitance and a 90 V Surge Arrester, see the insect in the bottom left of Figure 9. A proposed scheme for the monitoring of these voltages is given in Appendix B.

Even with this board we have the opportunity to perform the analog boundary scan with Rsens, GND1 and GND2. Nevertheless in this board the distinction of GND1 and GND2 has another function. Nodes Mon 1, Mon 2 and Mon 3, Mon x, are negative. In case the voltage to be monitored needs to be greater than zero, a positive offset voltage can be applied to GND1 that allows to shift the potential of nodes Mon x accordingly.

The board Type B can be used as Simple Board in Figure 6 if the 5 GΩ [6] monitoring resistors and Zmo’s are not assembled.

![Figure 9: Electrical schematic diagram of board Type B.](image)

6. Board Layout

Special precautions have been taken in the layout of the boards since the HVs into consideration must be confined in a relatively small space. In Figure 10 we can see the layout solution of board Type A (Type B is very similar). All the electrical tracks are buried under 0.8 mm of fiberglass that has a dielectric strength in excess of 40 KV/mm. The Printed Circuit Board, PCB has 4 layers.

In Figure 10 it is possible to observe the presence of cuts in the PCB around the critical soldering pins and critical track position. The cuts are peculiar in conjunction with the silicon rubber that is used to cover the board, as it will be explained below.
Both the board types populated, but not yet covered with silicon rubber are shown in Figure 11 and Figure 12.

The boards are covered with silicon rubber on both the top (18 mm of rubber thickness) and the bottom (10 mm of rubber thickness). Above the top and the bottom 2 shields (0.8 mm single sided PCB) cover the rubber.

Figure 10: Layout of the board Type A.

7. Board covering

Since the components that populate the boards are very close each other it is necessary to cover all with a material having a large dielectric strength. To this purpose we use the Silgard 3-4241 by Down-Corning having a dielectric strength in excess of 17 KV/mm [9]. The silicon rubber has been proved to be very suitable in application with HV [10], [11], [12].

Figure 11: Photograph of Type A board populated, but before being covered of silicon rubber.

We have a mould made of Aluminum covered by Teflon in which the board is put. The procedure adopted is as follow.

1. The boards are populated and cleaned;
2. The mould is filled with the silicon rubber and degassed in vacuum (to less than 0.2 mbar) for 15 min;
3. The board in the mould is cured at 60 °C for three hours;
4. The mould is opened and the board removed;
5. The board is finally cured (annealed) at 60 °C for 4 days. We have observed that due to the large thickness of rubber (about 20 mm) any residual ions that may give leakage solves after a long period at moderate temperature.

The final result of the cure is shown in Figure 13 and Figure 14. As can be seen in both figures the shields cover both the top and the bottom.

The importance of the cuts made around the critical electrical connections is visible in the cross section of the board in its final aspect, Figure 15. As it is put into evidence by the ovals the silicon is present all around the track, even in the direction parallel to the PCB surface, for at least 2 mm, the width of the cuts. This prevents any possible formation of surface leakage current that can generate discharges.

![Figure 12: Photograph of Type B board populated, but before being covered of silicon rubber.](image)

**8. Cable joining**

To join the HV cables from PCB to PCB and from PCB to HPD we have used 2 methods with similar results. The first method is based on the use of small brass cylinders inside which the 2 wires are soldered. The second method makes use of special crimped gold pins with about 2.5 mm diameters. In both cases after the wires are joined a insulating tube having enough thickness and length cover the joining point. In Figure 16 it can be seen an example with the tube being a commercial silicon having 2 mm of thickness.
9. Testing

To test the boards we take profit of the analog boundary scan in the configuration of Figure 17. We bias the board with -20 KV and measure the sum of the leakage current from the top, bottom and GND. To make this we connect GND1 to the ground of the HV power supply and measure the voltage that is developed across Rsens. An automatic test procedure performs the measurement cycling the HV up and down once per day. On a periodic scale the simulation of an HPD short circuited to GND is made. The HV is put down, a relays connects the 150 MΩ resistors to GND and the HV is again put up.

The test stays for a few days. A half-column can be verified at a time.

Figure 18 shows an example of characterization of the leakage current of a few boards that has been last for more than 6 days.

10. Radiation tolerance

The components used have been irradiated at the CERN facility during November 2004. Two boards populated and covered by the silicon rubber where subjected to irradiation. All the devices where subjected to fluence level of about $10^{12}$ n/cm$^2$, a secondary particle flux of $p$, $\pi^+$, $\pi^-$ between 0.3 and 4 GeV, and gamma from 100 KeV to 100 MeV.

It was not observed an appreciable change of the leakage current from the silicon rubber and the variation of any electrical components before and after irradiation was less than 10 %. It has to
be remarked that the dose considered is by far larger than that expected where the HPDs of the RICHx will be located.

Figure 15: Cross section of the board. Ovals are to indicate that the silicon rubber are all around the tracks.

Figure 16: Example of cable joint.

Figure 17: Set-up for the Type A board test. GND1 is connected to GND, GND2 is measured.
Leakage currents collected by the grounded nodes

Figure 18: Results of a characterization of a few boards that last for 6 days.

11. References


The high voltages will be monitored with the help of the well known ELMB boards. For each half-column we will monitor the voltage on the 3 focusing electrodes in the HPDs.

Appendix B: Monitoring of High Voltages (DRAFT from DCS group)

The high voltages will be monitored with the help of the well known ELMB boards. For each half-column we will monitor the voltage on the 3 focusing electrodes in the HPDs.
As already discussed these high voltages are reduced by a factor of 20000 by resistive divider contained in the HV boards and brought to the safe interval of $0 \text{V} \div -1 \text{V}$. The output voltages are carried to the ELMBs via a bifilar cable (specify) and connected to the differential input of the ELMB to avoid any possible ground loop.

The ELMBs are controlled by the PVSS system and use the FRAMEWORK tools developed at CERN by the JCOP group. The Rutherford lab group in LHCb has already successfully developed a preliminary software system to read these boards.

The schematic block diagram is shown in Figure 19.

**Figure 19: Proposed scheme for column monitoring.**