THE CUORE COLLABORATION

THE ESSENTIAL OF THE READOUT

ELECTRONICS OF CUORE

(Preliminary version V1)

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CLAUDIO ARNABOLDI
GIANLUIGI PESSINA

INFN di MILANO-BICOCCA
P.ZA DELLA SCIENZA 3
20126 MILANO-I

CLAUDIO.ARNABOLDI@MIB.INFN.IT
GIANLUIGI.PESSINA@MIB.INFN.IT
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1. Introduction

In this report we will very briefly describe the electronics foreseen for the experiment CUORE. Then, a description will be given of the communication protocol and the structure of the parameters addressing method with which the Electronic itself can be fully controlled remotely. In Appendix B some papers listed in the references are included to better describe the set up.

In CUORE there will be six different type of electronics equipments: the Front-End boards, the Bessel and Trigger boards, the Pulse generator boards, the High Performance Power Supplies and the Front-End boards for Temperature Stabilization. The Power sources Monitoring and Control are the cards units that control the operating condition of the pre-regulator power supplies.

A set of hubs are foreseen to distribute the communication between the computer and the final destination boards.

In the following, many features proposed for CUORE has been already tested and are currently running in the prototype experiment CUORICINO.

2. Description of CUORE electronics equipments and boards

2.A The very Front-End boards

The very front-end electronics will be located in the so called ‘19” rack’. Each 19” rack will accept 12 very Front-End boards [1], [2], [3], [4] to serve 24 detector channels (2 complete analog channels are on each board). Eight towers, or crates, composed by 6 racks each will be distributed around the cryostat. For the Front-end Electronics the total number of readout channels will be 8x(5.5)x12x2 = 1056.

The factor 5.5 indicate that one of the rack in any tower will be equipped with only half of the Front-End boards.

Every front-end board consists in a low noise and, very important, very low drift differential voltage sensitive preamplifier (Si JFETs input) having a fixed gain. The preamplifier operates at room temperature. An option is foreseen that include the presence of a differential buffer stage at cold (Si JFET) between the detector and the preamplifier. Much study has been made to face also this solution [5], [6], [7]. 24 detector channels are currently readout with such a configuration in CUORICINO.

A second stage has a programmable gain and follows the preamplifier. Since the system is DC coupled (the signal bandwidth is very small in our detectors), the offset voltage is made adjustable. The output of this chain is differential and drives a twisted cable up to the filtering stage, close to the DAQ. The differential signals are in groups of 12 and standard, low cost, 25 pin ‘D connectors’ are used for the connections.

The front-end boards provide also the biasing for the detectors. The load resistors [8] and the bias adjust circuit are provided from the board itself. Both the optimum operating condition and the detector characterization [9] can be performed. Channels with the cold buffer stage option have the load resistors at cold, too.
2.B  The Bessel and Trigger boards

In the tentative solution that follows, the one used for the CUORICINO experiment, every signal of the very front-end is split in 2 different analog signals that differ in amplitude and bandwidth. The Bessel and Trigger boards perform the splitting, the amplification and filtering. The signals generated within these boards are sent to the DAQ: one signal drives the ADC, the other the corresponding trigger [10], [11] input.

The Bessel and Trigger boards allocate 3 of such circuits each.

A single 19” rack could accept up to 16 Bessel and Trigger boards to serve 48 detector channels. For the filtering and triggering purpose 22 racks will be used corresponding to 22×16×3 = 1056 channels. They will be allocated close to the acquisition system, the DAQ.

The signal coming from the front-end board is filtered with a 6 poles (120 DB roll-off) active Bessel filter and sent to the ADC. The signal sent to the trigger of the DAQ is taken from the Bessel output, AC coupled to a programmable gain stage and further filtered with a 2 poles Bessel filter. In addition this circuit is provided with a special base line restorer and a pole-zero cancellation network that avoids any possible re-trigger coming from those large signals that could present undershot.

The connection between the Bessel and Trigger boards and the DAQ is made by means of appropriate twisted cables.

2.C  The Pulse Generator boards

To verify the drift of the energy conversion gain of the whole detector array, CUORE needs from 250 to 500 independent pulse generators. The total amount of pulse generators will depend on the grouping method selected for the heater resistors glued on each crystal. The output of every pulse generator is able to drive up to 8 heater resistors connected in parallel.

A single pulse generator board has four independent, not synchronous, outputs [12]. A rack equipped with 12 pulse generator cards will produce 12×4=48 signals. Adding a further rack per tower filled with pulse generators cards makes available 8×48=384 independent signal pulses.

The pulse generator has been designed and built for having less than 1.5 ppm/°C absolute drift. It can generate signals programmable in amplitude and width. Any pulse is generated only after having received a hardware trigger, to allow tagging. This trigger signal (implemented with a fiber optic) is dedicated, not included in the communication bus.

2.D  The High Performance Power Supplies

The Front-End boards, the Pulse generator boards and the Bessel and Trigger boards will be supplied by a Special Power Supply, SPS [13]. These equipments will be installed in each front-end rack and in each pulse generator rack. The total amounts of racks that need SPSs are at least 8×7+22 = 88.

The SPS has a very large power supply rejection ratio, low noise and very small drift, less than 4 ppm/°C.

2.E  The Power sources Monitoring and Control

To supply all the SPSs we plan to use 16 pre-regulators (actively filtered low noise switching type). It is foreseen a control system to monitor and control their operation.
2.F The Temperature Stabilization System.

The stabilization of the base temperature of CUORE detector holding towers will be controlled by simply exploiting some dedicated front-end channels [14]. The front-end channels that will be used for the stabilization will be based on the same hardware of the detectors readout, but they will be identified by the software system with a special ID code, in the virtual channel 0, and will be operated in a protected mode (commands repeated twice for any write operation) to prevent unwanted changes of the system temperature.

The stabilization system provides a large degree of accuracy. In the second phase of the experiment CUORICINO the main bath, the reservoir of the liquid Helium, is completely refilled every 2 days. The maximum observed residual drift of the detector baseline between two consecutive refills is less than 0.8 keV/day.

3. Description of the parameters addressing method

As described at the beginning of this document, the electronics of CUORE is located in racks. The racks will be piled up or located in towers. To avoid ambiguity the position of any channel is given by 4 addresses: the channel within the card, the relative position of the card within the rack (this is unambiguously indicated by the back plane present in the rack), the position of the rack within the tower and the address of the tower itself.

We summarize the parts that constitute a typical addressing structure for any device channels:
- **Tower** (of rack), for the communication protocol foreseen it is limited in range from 0 to 15.
- **Rack**, for the communication protocol foreseen it is limited in range from 0 to 15.
- **Board**, for the communication protocol foreseen it is limited in range from 0 to 15.
- **Channel**, for the communication protocol foreseen it is limited in range from 0 to 15.

To the above parameters used to address any device channel we have to specify which settings must be written or queried. This is specified by:
- **Byte Address**, for the communication protocol foreseen it is limited in range from 0 to 15.

The defined protocol is foreseen to handle 8 bits of configuration data:
- **DATA** (single byte) to be set in a write operation or read.

The described protocol is valid for all the boards of CUORE. Some differences are obviously applied to the **Channel** and **Byte Address** due to the different structure and feature that are found in them.

4. The virtual device at channel address 0

The front-end of CUORE will be constituted of boards featuring different tasks and having from one to four individual units inside them. These units are addressed within the boards starting from 1. The address 0 is left to individuate a virtual channel where all the information needed to identify the board type, its history and its states are stored.

We give a summary description of the configuration bytes of CUORE electronics. A detailed list is given in the last section of this document.
The virtual channel 0 of each board contains the common parameters and flags of the selected board.

The **Byte at address 0** is the device ID that identifies the hardware characteristics of the card. For instance, this number is also used to distinguish the generic front-end used for channel reading from the one used for temperature stabilization.

The **Bytes at addresses 1 and 2** contains the board serial number.

The **Byte at address 3** is used to identify the general status of the board.

The meaning of its bits is the following:
- Bit 0: Micro reset: used to force the reset of the micro controller of the devices
- Bit 1: Micro watchdog reset flag: used to identify a watch dog reset
- Bit 2: Micro brownout reset flag: used to identify a brownout reset
- Bit 3: Micro power on reset flag: used to identify the power on reset
- Bit 4: Board over temperature flag: used to identify the over temperature condition
- Bit 5: Board error flag: used to report an error condition
- Bit 6: Board warning flag: used to report a warning condition

From the **Byte at address 4** the temperature of the μ-controller (similar to the board temperature) is read.

In **Byte address 5** the level of the warning temperature can be written.

The implementation of thermal control depends on the μ-controller used and it could be unimplemented.

### 5. Front-end board channel parameters

The front-end board has two independent channels, each one individually addressable.

Up to now there are foreseen 12 bytes for the configuration of each front-end channel.

We start describing the **Byte at address 0**.

Two bits are dedicated to the loading of one of two default sets up stored in the board. For safety reasons, this command must be repeated twice to be executed.

The AUX OUT and TERMO OUT bits are used to select a signal to be connected to the Auxiliary Output. The signal may be either the analog output or the voltage of the analog thermometer located on the preamplifier.

The Auxiliary Output is a differential signal line that is common to all the channels, or groups of many channels. As a consequence only one channel can loads this line at a time. The software must account this constraint.

The SIGNAL TEST INT./EXT. bit is used to select the source for the test signal. The test signal is used to characterize and verify the operation of the full front-end chain, from the preamplifier to the ADC acquisition system.

The R CHAR./R MEAS. bit is used to select one from two pairs of load resistors. R CHAR. is for the bolometer characterization (for CUORICINO it is a pair of 5.45 GΩ connected to a bipolar bias voltage source). R MEAS. is the working load resistor (for CUORICINO it is a pair of 27 GΩ connected to a bipolar bias voltage source). This parameter will be unnecessary for the cold electronics readout, because in that case the load resistors are fixed and put at cold.
The GND - SIGNAL TEST /DETECTOR bit controls the connection of the preamplifier input. The GND - SIGNAL TEST option allows to connect the preamplifier to the signal test node or to a pair of 1 MΩ reference resistors for the measurement of the current that is flowing into the load resistors. The DETECTOR option forces the connection of the preamplifier to the detector, the normal mode of operation.

The last bit is the OFF-ADJ. If set, an auto-procedure starts that auto-adjust the output offset voltage at the level indicated in the byte at address 8.

The **Byte at address 1** configures the gain of the programmable gain amplifier. Not all its eight bits will be exploited.

The **Byte at address 2** configures the bias voltage attenuation of the programmable attenuator. Not all its eight bits will be exploited.

The **Byte at address 3** configures the common mode voltage for the detector bias. Not all its eight bits will be exploited. This configuration eventually will be stored in the board firmware and not available to the user. This correcting voltage allows compensating for any unbalance coming from the tolerance of the two load resistors that could produce a DC common mode voltage.

The **Bytes at addresses 4 and 5** take care of the amount of correcting currents injected in the proper nodes of the preamplifier to adjust the preamplifier output offset to the target value stored at Byte address 8.

The **Bytes at addresses 6 and 7** are used to control the test signal generator, for the auto-calibration of the front-end chain. In this preliminary version the operation of the test signal generator is not yet defined.

The target output offset voltage of the preamplifier is stored at **Byte address 8**. This target voltage is auto-imposed at the preamplifier output when the bit OFF-ADJ is set.

**Bytes at addresses 9, 10 and 11** contain the value of the voltage measured, with 24 bits of resolution, at the output of the board. When Byte at address 9 is queried the voltage is measured before the answer is given. The control software should take into consideration to stay in a wait state for a while, before the data are available.

### 6. Bessel and Trigger board channel settings

The board for the filtering and the analog preprocessing of the trigger signals has only **one configuration Byte** for each of its three channels. The described solution coincides with the one adopted for the experiment CUORICINO.

The first bit is set after the user has pushed the front-panel switch to manually loads one of the two default loadable configurations. Probably for CUORE this switch will be unassembled and controls will be managed only by software.

The ON/OFF bit allows bypassing the filter. This option is useful to check for the presence of any residual electromagnetic interference.

Two bits are for the bandwidth selection.

Two bits are for the pole-zero cancellation selection of the trigger output.

Two bits are for the gain selection of the trigger output.
7. Pulse generator board parameters

The pulse generator board has only one channel address and can manage up to four groups of heaters.

The **first Byte** stores the signal width expressed in units of 100 µs.

The **second Byte** and half of the third are used to select the signal amplitude. This is the signal amplitude present before an output attenuator and is controlled by a 12 bits DAC that uses a 5 V reference generator.

The four most significant bits of the third byte are necessary to select the output to be fired and to enable the pulse generation.

The **last Byte** is used to control the attenuation at each output and permit the selection of one value between four.

Once all the parameters and the enable bit are set, the pulse generator waits to be fired by a synchronizing triggering at a dedicated input, independent from the communication bus. The link for this input is a fiber optic.

The generation of a pulse at any of the four selected outputs needs the reconfiguration of the above parameters and the generation of a new synchronizing trigger.

The operation of the pulse generator described coincides with the one used for CUORICINO.

8. The High Performance Power Supply configuration

The high performance power supply will have two or three outputs.

Two outputs will be the low noise and high stability bipolar analog outputs (±5 V to ±10 V, selectable) and the third one will be dedicated to the digital power supply.

The controls for each output are of the same types, the only difference is in their channel address.

The **Byte at address 0** is used to queried the loading of one of the two settings (for a single output voltage or for both outputs) stored in the flash memory, or for checking the error flags.

The **two Bytes at addresses 1 and 2** are used to set the output voltage.

The **Byte at address 3** is used to read the output current.

The **Bytes at addresses from 4 to 8** are used to configure the limits for the output current and the warning levels for the input voltage, for the output voltage or for the output current. The warning levels define when the internal control logic has to wake up to verify an incorrect condition.

The output voltage is limited for the safety of the load. The output current limit and the voltage warning levels are limited for the safety operation of the power supply.

9. PC interface and device drivers

The physical connection between the Control System, a PC, and the hardware, will be based on one or more serial RS232 ports. The PC serial ports will use the Xon/Xoff handshake or the hardware one.

The speed has to be defined.
The data will be exchanged using packets that will include an identification number that
individualizes which PC task has generated them, and the address of the selected hardware.

An optical fiber link will connect the PC to some hubs that will distribute the packets to the
final destination boards.

A μ-controller unit present on the device will manage the transmission, store the settings and
execute the commands.

Some software functions will be provided that allows to decode all the setting bytes in analog
parameters.

10. References

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11. APPENDIX A: Tables of the configuration parameters

11.A The Front-End board parameters

**Channel 0:**
- Byte Add. 0:
  - 8 bits for Front-End type ID (Read Only, RO)
- Byte Add. 1:
  - 8 bits for MSBs Front-End board serial number (RO)
- Byte Add. 2:
  - 8 bits for LSBs Front-End board serial number (RO)
- Byte Add. 3:
  - 8 bits to check from common errors (Slow polling)
    - Micro reset
    - Micro watchdog reset flag
    - Micro brownout reset flag
    - Micro power on reset flag
    - Board over temperature flag
    - Board error flag
    - Board warning flag
    - ...
- Byte Add. 4:
  - 8 bit for board temperature measurements (RO)
- Byte Add. 5:
  - 8 bit for board over temperature level set (Read/Write, R/W)

**Channel 1..2:**
- Byte Add. 0:
  - 1 bit to command the load of default status A
  - 1 bit to command the load of default status B
  - 1 bit for AUX OUT
  - 1 bit for TERMO OUT
  - 1 bit for SIGNAL TEST INT. / EXT.
  - 1 bit for R CHAR./R MEAS.
  - 1 bit for DETECTOR / GND - SIGNAL TEST
  - 1 bit for OFF-ADJ (auto-offset adjustment, the target voltage is at Byte address 8)
- Byte Add. 1:
  - 8 bits for GAIN set
- Byte Add. 2:
8 bits for BIAS set

Byte Add. 3:
8 bits for BIAS CM. set

Byte Add. 4:
8 bits for MSBs of the displacement to be added to an internal node of the preamplifier to adjust the preamplifier output at the target voltage of Byte at address 8
(while writing the MSB the LSB stay unaltered)

Byte Add. 5:
8 bits for LSBs of the displacement to be added to an internal node of the preamplifier to adjust the preamplifier output at the target voltage of Byte at address 8
(while writing LSB the MSB stay unaltered)

Byte Add. 6:
3 bits for SIGNAL TEST CONFIGURATION
5 bits for SIGNAL TEST TYPE

Byte Add. 7:
8 bits for SIGNAL TEST AMPLITUDE

Byte Add. 8:
8 bits for output voltage target offset. This voltage is auto-imposed at the preamplifier output when the bit OFF-ADJ is set.

Byte Add. 9:
8 bits MSB of the 3 bytes where the measured output voltage is stored. This Byte should be queried first since the measurement is taken just at this time

Byte Add. 10:
8 bits MediumSB of the 3 bytes where the measured output voltage is stored.

Byte Add. 11:
8 bits LSB of the 3 bytes where the measured output voltage is stored.
11.B The Bessel and Trigger board parameters

**Channel 0:**
- Byte Add. 0:
  8 bits for Bessel and Trigger type ID (RO)
- Byte Add. 1:
  8 bits for MSBs Bessel and Trigger board s.n. (RO)
- Byte Add. 2:
  8 bits for LSBs Bessel and Trigger board s.n. (RO)
- Byte Add. 3: 8 bits for check from common error (Slow Polling)
  - Micro reset
  - Micro watchdog reset flag
  - Micro brownout reset flag
  - Micro power on reset flag
  - Board over temperature flag
  - Board error flag
  - Board warning flag
  - ...
- Byte Add. 4:
  8 bit for board temperature measurements (RO)
- Byte Add. 5:
  8 bit for board over temperature level set (Read/Write, R/W)

**Channel 1..3:**
- Byte Add. 0:
  1 bit flag for manually loaded default configuration (CUORICINO HW)
  1 bit for filter bypass
  2 bits for bandwidth
  2 bits for pole-zero compensation
  2 bits for trigger gain
11.C The Pulse Generator parameters

**Channel 0:**

Byte Add. 0:
- 8 bits for pulse generator type ID (RO)

Byte Add. 1:
- 8 bits for MSBs pulse generator board s.n. (RO)

Byte Add. 2:
- 8 bits for LSBs pulse generator board s.n. (RO)

Byte Add. 3:
- 8 bits for check from common error (Slow Polling)
  - Micro reset
  - Micro watchdog reset flag
  - Micro brownout reset flag
  - Micro power on reset flag
  - Board over temperature flag
  - Board error flag
  - Board warning flag
  - …

Byte Add. 4:
- 8 bit for board temperature measurements (RO)

Byte Add. 5:
- 8 bit for board over temperature level set (Read/Write, R/W)

**Channel 1:**

Byte Add. 0:
- 8 bits for pulse width

Byte Add. 1:
- 8 bits for LSBs amplitude

Byte Add. 2:
- 4 bits for output selector and pulse enable
- 4 bits for amplitude MSBs

Byte Add. 3:
- 2 bits for attenuation selection on channel 4
- 2 bits for attenuation selection on channel 3
- 2 bits for attenuation selection on channel 2
- 2 bits for attenuation selection on channel 1

NOTE: the pulse generator has an additional trigger input, different from the communication bus, for pulse synchronization.
11.D  The High Performance Power Supply parameters

Preliminary version.

**Channel 0:**

Byte Add. 0:
- 8 bits for power supply type ID (RO)

Byte Add. 1:
- 8 bits for MSBs power supply serial number (RO)

Byte Add. 2:
- 8 bits for LSBs power supply serial number (RO)

Byte Add. 3:
- 8 bits for check from common error (Polling required, important)
  - Micro reset
  - Micro watchdog reset flag
  - Micro brownout reset flag
  - Micro power on reset flag
  - Board over temperature flag
  - Board error flag
  - Board warning flag
  - ...

Byte Add. 4:
- 8 bit for board temperature measurements (RO)

Byte Add. 5:
- 8 bit for board over temperature level set (Read/Write, R/W)

**Channel 1:**  // Analog Positive output

Byte Add. 0:
- 8 bits for common controls
  - 1 bit to command the load of default status A
  - 1 bit to command the load of default status B
  - Positive output error flag
  - Positive output warning flag
  - Positive Over voltage flag
  - Positive Under voltage flag
  - Positive Over current flag
  - Positive Under current flag
  - ...

Byte Add. 1:
- 8 bits for MSBs of Vout. *1

Byte Add. 2:
- 8 bits for LSBs of Vout. *1
Byte Add. 3:
  8 bits for output current 
  
Byte Add. 4:
  8 bits for Over_Current_limit 
  *2

Byte Add. 5:
  8 bits for Over_Voltage_Input warning level 
  *2

Byte Add. 6:
  8 bits for Under_Voltage_Input warning level 
  *2

Byte Add. 7:
  8 bits for Under_Voltage_Output warning level 
  *2

Byte Add. 8:
  8 bits for Over_Current warning level 
  *2

Byte Add. 9:
  8 bits for 

Channel 2: 
  // Analog Negative output

Byte Add. 0: 8 bits for common controls
  - 1 bit to command the load of flash status A
  - 1 bit to command the load of flash status B
  - Negative output error flag
  - Negative output warning flag
  - Negative Over voltage flag
  - Negative Under voltage flag
  - Negative Over current flag
  - Negative Under current flag
  - ....

Byte Add. 1:
  8 bits for MSBs of Vout. 
  *1

Byte Add. 2:
  8 bits for LSBs of Vout. 
  *1

Byte Add. 3:
  8 bits for output current 
  (RO)

Byte Add. 4:
  8 bits for Over_Current_limit 
  *2

Byte Add. 5:
  8 bits for Over_Voltage_Input warning level 
  *2

Byte Add. 6:
  8 bits for Under_Voltage_Input warning level 
  *2

Byte Add. 7:
  8 bits for Under_Voltage_Output warning level 
  *2

Byte Add. 8:
  8 bits for Over_Current warning level 
  *2

Byte Add. 9:
Channel 3: // Digital output (3.3 V or 5 V) (Only if implemented)

Byte Add. 0: 8 bits for common controls
- 1 bit to command the load of flash status A
- 1 bit to command the load of flash status B
- Digital output error flag
- Digital output warning flag
- Digital Over voltage flag
- Digital Under voltage flag
- Digital Over current flag
- Digital Under current flag

Byte Add. 1:
8 bits for MSBs of Vout. *1

Byte Add. 2:
8 bits for LSBs of Vout. *1

Byte Add. 3:
8 bits for output current (RO)

Byte Add. 4:
8 bits for Over_Current_limit *2

Byte Add. 5:
8 bits for Over_Voltage_Input warning level *2

Byte Add. 6:
8 bits for Under_Voltage_Input warning level *2

Byte Add. 7:
8 bits for Under_Voltage_Output warning level *2

Byte Add. 8:
8 bits for Over_Current warning level *2

Byte Add. 9:
8 bits for ..... 

*1 These values could be limited by the power supply firmware for load safety operation.

*2 These values could be limited by the power supply firmware for its safety operation.
12. APPENDIX B: some papers listed in the references

Reference [1]:

A Low Dc Drift Read-Out System For A Large Mass Bolometric Detector

A.Alessandrello, C.Brofferio, C.Bucci, D.V.Camin, O.Cremonesi, A.Giuliani, A.Nuccioiti, M.Pavan, G.Pessina, E.Previtali and G.Sablich
Istituto Nazionale di Fisica Nucleare and Dipartimento di Fisica dell'Università Via Celoria 16, 20133 Milano, Italy

Abstract

We present a read-out system for large mass bolometric detectors. It consists of a differential voltage-sensitive preamplifier having very low series and parallel noise, thanks to the use of a pair of selected silicon JFET at the input. Very good electrical characteristics were obtained. DC power supply rejection ratio, thermal drift of input offset voltage and input leakage current are minimized by using novel circuit solutions. Parallel noise behavior was also investigated using a new measurement method which is sensitive to the shot noise generated by very small currents (tens of nA).

I. INTRODUCTION

A large mass bolometric detector consists of two parts. 1) An energy absorbing crystal cooled to very low temperatures, (~10 to 100 mK) to get minimal heat capacity. In this way an energetic particle which impinges onto the crystal, releasing all or part of its energy, is able to increase the temperature by a measurable amount, inversely proportional to the heat capacity itself. 2) A temperature sensor, a thermistor in our case, put in good thermal contact with the crystal, converts the temperature increase into an electrical signal, read-out by a low-noise preamplifier. The thermistor has a static resistive impedance, in the tens to hundreds of MΩ range. Its dynamic component shows also an inductive effect [1].

During the last few years we have progressively increased the mass of our detectors [2], with the consequent shift of the signal energy spectrum toward lower frequencies, down to a few tens of Hz. The low parasitic capacitance of cold electronics, previously used [3], was no longer required, as now the detector resolution is not affected by large stray capacitances.

These detectors, which can reach in principle a very high energy resolution [4], can be read-out by a fully DC coupled system or, alternatively, they can be AC biased, in which case the slow signal will amplitude-modulate the sinusoidal bias voltage across the thermistor. An AC bias system is presently under study. The DC bias approach, subject of this paper, requires a read-out with low series noise at low frequencies and low parallel noise. This is necessary to process detector signals contained in bandwidth of a few tens of Hz, as those developed on the large resistive impedance of the detector. Energy conversion gain variations are always present, possibly generated by slow thermal drift of the cryogenic system. The read-out system can be sensitive enough to these fluctuations if it has a very low drift.

It can be shown that under the usual working conditions of our large mass bolometers, the parasitic capacitance shunting the thermistor has effects on the energy resolution performances only when it becomes of the order of hundreds of pF [5]. A read-out system with the preamplifier put outside the refrigerator, a few meters away from the detector, could in principle be a practical solution. A possible drawback could come from the microphonic noise due to the vibrations of the connecting link, proportional to the length of the wires. Still this common mode noise can be minimized by adopting a differential configuration for the preamplifier.

In this paper a new Differential Voltage-Sensitive Preamplifier (DVSP) designed for the read-out of an array of 20 TeO₂ bolometers, 330 g each, is described. To obtain both very low parallel and 1/f series noise, a pair of silicon JFETs has been used at the preamplifier input. Although a discrete preamplifier has been realized, very good dynamic and static performances have been obtained, very close to that achievable with good monolithic circuits. This was possible by using non standard circuit configurations.

In the following sections the steps for the development of the complete DVSP will be described. The DVSP drift voltage was minimized by implementing a very large DC Power Supply Rejection Ratio (PSRR), as described in section II, and a very low thermal drift, section III. In particular the low thermal drift was obtained thanks to the use of a new compensation procedure. In section IV the study of the static and noise behavior of the input leakage current is illustrated. Results were used to optimize the bias of the input JFETs. In the same section a new method which allows to measure parallel noise at very low levels is illustrated as well. In section V the complete circuit of the preamplifier is shown and described. Finally section VI describes the temperature stabilization and cooling of the input JFETs of the DVSP, necessary to minimize the input leakage current.

II. PREAMPLIFIER REJECTION TO POWER SUPPLY

We firstly describe the Power Supply Rejection Ratio (PSRR) which at DC must be very high to minimize the baseline fluctuation in the data acquisition system. The DVSP shows a PSRR of about 75 dB. To increase it further we decided to implement a very stable voltage supply based on the BB REF-102 device, a monolithic 10 V reference voltage chip, having 1 ppm/°C drift and 110 dB of PSRR. Its output voltage was buffered to be able to drive a current of about 150 mA, or 5 preamplifiers. By using two such devices and two
buffers, a symmetric ±10 V supply voltage was obtained. To measure the DC PSRR, the supply voltages (±12 V) of the REF102 and buffer system were varied in small steps, at intervals of about 4 min each, obtaining a triangular wave of 2 hs period and 1 V amplitude. LabView software was used to modulate the supply voltages (adding the offset of an HP3314A signal generator to a ±12 V floating voltage source) and to measure both the supply voltage and the preamplifier output with an HP3478A multimeter, whose input was multiplexed by means of two relays.

The supply voltages were varied one at a time. PSRR was determined by finding correlation between the shape of the applied signal and the DVSP output, after the DVSP reached the stabilization (~5 hs). The estimated sensitivity of the measurement chain was about 147 dB. The negative (−12 V) supply PSRR was determined to be 146 dB, while for the positive supply we obtained 137 dB. Figure 1 shows the measurement results. The DVSP voltage gain was 218.

III. THERMAL DRIFT SUPPRESSION

The DVSP offset voltage drift must be as small as possible, to be able to monitor variations in the signal baseline. Small drift is not simple to be realized in general, and in particular when a preamplifier is implemented with discrete components, as in this case. The standard approach would be to look for good thermal matching of the sensitive devices. We have adopted a different approach, based on practical considerations, as described below.

The thermal drift in a limited temperature range has a linear dependence with temperature. This is the case with discrete metal film resistors or base-emitter or gate-source voltages of transistors. Let’s assume, for the moment, that a possible imbalance of the input leakage currents does not generate a measurable offset voltage on the source input impedance. We then expect that if a mismatch between components inside the circuit is present, the preamplifier output voltage changes linearly with temperature.

Instead of looking for the source of the mismatch, the adopted solution tries simply to compensate for the existent drift. For that purpose a voltage or current source Proportional To the Absolute Temperature (PTAT) must be realized. The principle of operation of the adopted solution is illustrated in figure 2. A 2 μA/°C current generator, whose circuit implementation is described in detail in section V, was realized. Regulation of trimmer T2 permits to add an amount of thermal current, with a polarity opposite to the unwanted present drift, in proper differential nodes of the preamplifier circuit.

![Figure 2: Schematic diagram of the PTAT current generator.](image)

The results obtained were satisfactory. A preamplifier input voltage drift of 0.5 μV/°C was obtained as a typical value. The lowest drift was 0.1 μV/°C. Figure 3 shows the input offset voltage recorded over a few days, showing the long term stability of the system. The room temperature, following the laboratory conditioning system, is also shown. LabView was used to read, every 3 minutes, the DVSP output and a platinum resistive thermometer. The average drift is about 0.5 μV/°C, which becomes 0.7 μV/°C if we consider that during the day doors are continuously opened and closed, (setting sharp changes of room temperature) and people move around. It must be noted that without the correction circuit, the thermal drift of the preamplifier alone was never less than 10-30 μV/°C.

![Figure 3: DVSP input drift vs room temperature.](image)

IV. INPUT LEAKAGE CURRENT STUDY

The input leakage current may create two important effects: parallel noise and offset voltage across the source input impedance (if there is an imbalance between the two bias currents). Leakage current was studied in two steps. Firstly we looked for a dependence on the reverse drain to gate and source to gate voltages, to optimize the bias of the input JFETs. Secondly, a measurement of the parallel noise as a function of the static measured leakage current was made, to investigate for effects other than the expected pure white shot

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noise. For both measurements special set-ups were implemented.

A. Static Measurement of the Leakage Current

Input leakage currents (I_{LE}) of input JFET transistors are due to the gate-to-channel junction reverse voltage. The dependence of I_{LE} on the junction reverse voltage is expected to follow the law [7]:

\[ I_{LE}(T, V_R) = I_S(V_R) \exp \left( \frac{-E_G}{\eta k_B T} \right). \]

(1)

In eq.(1) E_G is the silicon energy gap, k_B the Boltzman constant and T the absolute temperature. \( \eta \) is a parameter which is equal to 1 when the dominant current is of diffusion type, 2 when it is of generation-recombination (G-R) type. In the latter case the saturation current I_S will depend on the width of the depletion region which, in turn, depends on the reverse voltage, V_R, with a law which is a function of the doping profile. In silicon, at low doping concentration, like those used for the channel of JFETs, the G-R current is dominant and a dependence on the reverse voltage is expected.

We have investigated this dependence in order to optimize the drain to source voltage of the input transistors, Toshiba 2SK146. For the measurements the device was configured as a diode, with the drain and source connected together. A special procedure was implemented to correct for the offset current of the reading circuit. The set-up is shown in figure 4. To compensate for the input leakage current, I_{LE}^{DUT}, during the measurement, we added a diode J_1, adjusting its reverse voltage V_{COMP} to force I_{COMP} to be equal to I_{LE}^{DUT}, while switch SW is open. The condition I_{COMP}=I_{LE}^{DUT} is reached when the output voltage is stable. In this way, after closing SW, the output voltage is expected to depend only on I_{LE}. The capacitance C_{INT} is then charged with I_{LE}. The time interval between two different reference values of the output voltages is inversely proportional to I_{LE}.

The current was measured as a function of both reverse voltage and temperature. Temperature was varied in steps of \( 10 \, ^\circ \text{C} \), from room temperature to about \(-20 \, ^\circ \text{C} \), using a Peltier cell to cool the JFET transistors.

Data and interpolations are shown in figure 5, and interpreted as follows. A clear dependence of I_{LE} on the reverse voltage is observed, suggesting that the current is of G-R type. A G-R current becomes constant when the width of the depletion region equals the physical junction region. For a JFET this happens at voltages comparable to the pinch-off voltage which, for the present case, is less than 1 V. A possible explanation of why in figure 5 I_{LE} increases for reverse voltages greater than 1 V could be that these devices have the substrate, lightly doped p-type, connected to the effective gate. When the reverse voltage is increased the depletion region extends deeply into the substrate, increasing I_{LE}. The dependence of the measured current on the voltage was close to linear (see figure 6), as already observed in literature [8].

At low temperatures I_{LE} tends to a finite value, instead of becoming negligible. We attribute this effect to a parasitic resistance, R_{PAR}, due to the JFET itself, or to the integrating capacitance used for the measurement. An estimate of its value was extracted by assuming that at the lowest temperatures reached, I_{LE} was due only to R_{PAR}, regardless of the reverse voltage, in the range considered. The data interpolation is shown in figure 7: the resulting resistance is 15 \( \Omega \).

The indication that the current is of G-R type and the presence of a parasitic resistance were taken into account to find the final interpolation functions shown in figure 5. The actual function used for the interpolation was (see also eq.(1)):

\[ I_{LE}(T, V_{DG}) = I_S(V_{DG}) \exp \left( \frac{-E_G}{\eta k_B T} \right) + \frac{V_{DG}}{R_{PAR}}. \]

(2)

Fits of the data returns E_G/(\eta k_B)=6385 K, in good agreement with the theoretical value.
agreement with the theoretical value of 6667 K, for G-R type current behavior. Measurements accuracy can be seen as well normalizing all data with the leakage current measured at room temperature, to be independent from the reverse voltage. From eq. (2) a new dimensionless function $y_{LE}(T)$ can be introduced which satisfies:

$$y_{LE}(T) = \frac{I_{LE}(T, V_{DG}) \cdot \frac{V_{DG}}{R_{PAR}}}{I_{LE}(300K, V_{DG}) \cdot \frac{V_{DG}}{R_{PAR}}} = \exp \left( \frac{-E_G}{\eta K_B T} \right). \quad (3)$$

As can be seen in figure 8 all the normalized data fits very well with interpolation.

The leakage current for these devices is very low when bias voltage is fixed to be less than 1 V, which is a limiting operating point to get good dynamic characteristics. Moreover, if the temperature of operation is fixed around 0 °C, or less, $I_{LE}$ is lower than 10 fA, becoming limited at most by a parasitic resistance of 15 TΩ. It must be noted that this resistance generates a parallel noise equivalent to a shot noise generated by a current of only 5 fA.

The same kind of measurements have been done with the devices connected as transistors at the input of the DVSP. No appreciable differences were observed in the dependence of the leakage current with temperature, compared to the diode configuration case.

**B. Input Parallel Noise Measurements**

Studies on parallel noise must be performed to understand whether its origin is pure shot noise of the leakage current (shot noise of G-R origin has Lorentzian components [9]), or if there are contributions also from other sources, like second stage or common mode disturbances.

A classical way to perform this test is to employ a bias resistor of large value to reference the preamplifier input to ground [10], [11]. Due to the low level of shot noise we want to investigate, generated by a current of less than 100 fA, we need at least 1 TΩ resistor, to have a negligible parallel thermal noise. Another approach is to implement a resonant circuit with capacitors and inductors at the preamplifier input,

to enhance parallel noise contribution in a tuned, narrow, frequency bandwidth [12]. Both methods are not suitable for the present application. The first one because of the very large value needed for the reference resistor, the second one because it is very difficult to get a low tuned frequency, close to DC, as we need.

![Figure 8: Normalized leakage current vs inverse of temperature.](image)

The adopted approach was instead very simple and efficient. A non dissipating input load impedance was used (a capacitance). Data was taken at different temperatures, looking for a correlation between measured noise and static current measurements. This way it was possible to separate shot noise effects from other sources of parallel noise, because the former depends exponentially on temperature, while other effects generally don’t, especially if the only cooled device is the JFET itself.

The set-up implemented is an elaboration of a method already adopted for a solid state detector biasing [13], where a reverse biased diode is used to load and compensate for the detector leakage current. For the present case we have used a “diode connected” JFET, similar to the one located at the preamplifier input, to feedback the preamplifier (figure 9). In this way the preamplifier input leakage current, $I_{LE}$, is forced into the feedback diode $J_F$, which biases itself in the reverse region, with a voltage close to the drain-to-gate voltage of the preamplifier input JFET, $V_D$. From here on, drain-to-gate and drain-to-source voltages are considered equal, because the transistors are operated close to the saturation current $I_{Ssat}$.

The reverse biased junction behaves as a capacitance ($C_F$) into which the leakage current is integrated. The noise of $J_F$ is

![Figure 9: Schematic diagram of the set-up used for the parallel noise measurement.](image)
the same as that of $J_I$: we expect to measure twice the parallel noise of the input transistor $J_I$. Output noise due only to parallel noise should be:

$$V_O^2 = \left( \frac{\alpha}{\omega \cdot C_F} \right)^2 \left( 2qI_{LE} \right)^2;$$

(4)

where $\omega$ is the angular frequency, and $\alpha(\omega)$ is a correction factor which takes into account the fact that the preamplifier is not ideal. Since the feedback capacitance $C_F$ depends on the diode bias condition, its value is not known "a priori". For this reason the actual frequency response is measured by injecting a test signal by means of a capacitance $C_T$ of known value:

$$T_F(\omega) = \frac{\alpha}{\omega \cdot C_F} \Rightarrow \frac{\alpha(\omega)}{\omega \cdot C_F} = \left( \frac{T_F(\omega)}{\omega \cdot C_T} \right)^2;$$

(5)

Both the noise and the frequency response were measured with the help of a dynamic signal analyzer HP3562A. The noise measured at the preamplifier output, using eq. (4), is referred to the input by means of the measured $T_F(\omega)$, given by eq. (5). By dividing also by the a factor 2(2q) an equivalent shot noise current is obtained. As an example figure 10 shows the equivalent input shot noise for $V_{DG}$ equal to 1 V, obtained at two different temperatures of operation: room temperature and -23 °C. As it can be seen, the equivalent noise is white in the frequency range considered. Measurements were taken at different temperatures and drain-to-gate voltages (1 V and 3 V).

So far the results obtained include both parallel noise and all the possible contributions to parallel noise coming from second stage and common mode signals. To discriminate between the two effects we looked for a correlation between measured noise and static leakage current. The correlation considered was:

$$I_{LEN} = I_{LE} + I_{LEN}(V_{DG}) + I_{HIST};$$

(6)

where $I_{LEN}$ is the total measured noise current, $I_{LE}$ is the static current measured as shown in section IV.A, $I_{LEN}(V_{DG})$ is a term which takes into account a noise behavior different from pure shot noise and, finally, $I_{HIST}$ is the possible contribution coming from second stage. Results obtained are shown in figure 11. It can be seen that there is a contribution for $I_{LEN}(V_{DG})$, of about 60 fA/V$_{DG}$ as a rough approximation. The cause is not yet understood. It can be excluded that this is related to the intrinsic voltage gain of the input transistors, otherwise the expected effect should be in the opposite sense. The induced, correlated noise coming from the channel [9] cannot justify the observed effect, either. A source of noise, of about 250 fA, independent of leakage current is also present at $V_{DG}=1$ V. This is mainly due to common-mode noise coming from supply voltages, which, in this circumstance, were not the ones adopted and described in section II. In this non-differential set-up only the shot noise of the input JFET were present, the equivalent input current for the mentioned source of noise would be two times larger (500 fA).

We will investigate further the behavior observed, by setting different drain to gate voltages. We also plan to improve this already extremely sensitive method, trying to realize a true differential parallel noise measurement, by connecting another diode at the second input of the DVSP.

So far it has been proved that when the JFETs are biased with $V_{DG}$ equal to 1 V and operated at a temperature lower than 0 °C, equivalent parallel shot noise has a pedestal of 60 fA, although leakage current becomes negligible. If not operated in true differential way, which is not the case for the present application, a supply voltage effect is observed which may increase the equivalent parallel noise to even 400 fA.

V. DVSP CIRCUIT DIAGRAM - NOISE PERFORMANCE

All the results described in the previous sections, have been taken into consideration for the design of the DVSP. The whole circuit is illustrated in figure 12. Use of a few Operational Amplifiers, OAs, has been adopted to obtain good symmetry. The circuit board is 2.5 X 3 cm$^2$; the input JFET can be mounted on the board, or far away, if cooled.

The pair of input transistors $Q_1$ and $Q_2$ is cascaded by the JFETs-OAs combination realized with transistor $Q_3$ and $Q_4$ and two OAs (3/4 and 4/4 of a quad TL074). The reference
voltage for the cascode combination is the virtual ground present at the middle point of the feedback resistors R₁ and R₆, connected at the sources of Q₁ and Q₂. In this way the drain to source voltages of Q₁ and Q₂ are fixed to 1 V, optimizing input leakage current, independently from the common mode input voltage. The cascode output is converted from differential to single-ended by the low noise OA OP27. The structure is feedback with the resistors R₅, R₆ and R₇, R₈. The resulting closed-loop voltage gain, given by \((1+R₅)/R₆\), is 218. It must be noted that the circuit has a high input impedance despite the use of only one pair of input transistors. Sink currents of 1 mA each for transistors Q₁ and Q₂ are given by the current generator formed with Q₆, R₈, and 1/4 of the TL074.

Final considerations concern the offset adjustment, and the PTAT operation. Since they must generate a common mode imbalance, great attention was put in their implementation, to avoid negative effects on both dynamic and noise performances. Output offset voltage adjustment is made through a current generator formed by Q₆, R₇, one OA (2/4 TL074) and the trimmer T₁. T₁ is connected to the circuit at nodes A and B, which, being of low impedance, avoids possible problems with asymmetry coming from non perfect balance of load impedances. Maximum current is about 250 \(\mu A\), with which a compensation of \(\pm 22 \text{ mV}\) of input DC differential voltage (i.e. the detector bias) is possible. To generate this low current, a large value resistor R₇ must be used. This assures enough degeneration for noise and drift of the current generator itself.

The same nodes A and B are used to feed the thermal offset current coming from the PTAT generator, composed by the monolithic reference source voltage LM35, which develops 10 mV/°C, and the two OAs (1/2 and 2/2 TL072). The two OAs convert the voltages at their inputs into two currents, one of each having a thermal drift of 2 \(\mu A/°C\) derived from the LM35. The resulting output current injected into the trimmer T₂ is the thermal current indicated in figure 2, plus a small offset current of about 10 to 20 \(\mu A\). The PTAT is therefore capable to compensate up to 360 \(\mu V/°C\) at the DVSP input. Non compensated DVSP input drift voltage is of the order of 10 to 30 \(\mu V/°C\). Since this is about 10 % of the PTAT current, only a small amount of it is needed to compensate the preamplifier drift, minimizing noise effects of the PTAT network.

Preamplifier series noise is shown in figure 13. At a frequency of 0.1 Hz the noise is less than 100 nV/√Hz. It rolls-off following a Lorentzian spectrum, as expected for a device having a single trap in the energy gap. At 1 Hz the noise is less than 30 nV/√Hz, and becomes 5 nV/√Hz at 10 Hz. Integrated noise between 0.1 and 10 Hz is less than 80 nV_{RMS}. With a detector energy conversion gain of about 0.9 mV/MeV, and a bolometer impedance of 520 MΩ, the equivalent energy noise due to the DVSP is 290 eV Full Width Half Maximum (FWHM), with 60 fA of input leakage current at each DVSP input. This result has to be compared

![Figure 12: Complete circuit for the Differential Voltage Sensitive Preamplifier DVSP.](image-url)
with the actual detector energy resolution of about 3 KeV FWHM [14].

As far as dynamic performances are concerned, the DVSP has a frequency bandwidth limited to a few kHz, and a Common Mode Rejection Ratio of about 85 dB from DC to about 1 KHz. Integral non linearity is 0.05 % for ±6 V output voltage swing, corresponding to ±27.5 mV variations in the differential input.

VI. TEMPERATURE STABILIZATION AND COOLING OF INPUT JFET TRANSISTORS

Input JFETs have a leakage current of about 330 fA at room temperature, which reduces to about 10 fA if the temperature is of the order of 0 °C. We therefore decided to lower the temperature of the JFETs. Since the experiment is located inside a Faraday cage, a DC ‘cooling’ system was realized, to avoid the introduction of line cables inside the cage. A 5.5 W power capability Peltier cell, capable to set a thermal gradient of ±65 °C, was placed on the floor of an hermetic metallic box. Two JFETs and two platinum thermometers were put in good thermal contact with the cell by means of a spring system. The metallic box was thermally connected to a heat sink, having 0.3 °C/W thermal resistance, and it was evacuated with a peristaltic pump, to reduce thermal contact between the Peltier cell and the laboratory environment. The minimum temperature registered by the thermometers in this configuration was -23 °C.

One of the two thermometers was used for stabilizing the temperature at -6 °C. The stabilization circuit is shown in figure 14. It is based on the use of the monolithic instrumentation amplifier BB IN130, able to feature a voltage gain of 10000 with an input offset drift voltage of less than 0.1 µV/°C. A double feedback was realized. The INA130 was made unity gain stable by adding a dominant pole, R2 C1. A driver was connected at the output, able to feed the suitable current to the cell (about 2 A). A capacitor C2, of very large value, was then added to give to the amplifier a unity gain frequency bandwidth of less than 4 Hz. This configuration guarantees that when the temperature of the cell is regulated, the resulting second feedback loop is stable.

Residual thermal conductance between the devices put on the cell, inside the box, and the laboratory environment was compensated by stabilizing the internal box temperature to a few degrees over room temperature. A heater, a long strip platinum thermometer and a circuit similar to that shown in figure 14 were used for the purpose. In this way the temperature of the devices on the cell reached a stabilization of 40 m°C/°C, while the temperature inside the box varies 100 m°C/°C. This condition was obtained at a temperature of -6.3 °C (see figure 15), where the leakage current is less than 10 fA.

When the input JFETs are cooled and stabilized, together with the box temperature, the DVSP is able to reach a thermal drift of less than 5 µV/°C, if the thermal drift compensation is not used. The result approaches the one shown in section III, if thermal compensation is put into operation.

VII. SUMMARY AND CONCLUSIONS

A Differential Voltage Sensitive Preamplifier (DVSP) capable to fulfill the specifications required to read out signals coming from a bolometric detector of large mass was realized. New circuit solutions and measurement methods have been implemented. Table 1 shows the performances obtained for the DVSP. Input offset voltage thermal drift was very low, despite the use of discrete active devices, thanks to a new circuit design, able to compensate for the preamplifier drift. The use of discrete input JFETs transistors permitted to obtain low series noise and input leakage current. Intensive experimental studies have been done on the leakage current

![Figure 13: Series noise of the DVSP.](image1)

![Figure 14: System for cooling and stabilization of the JFETs.](image2)

![Figure 15: Temperature of the devices on the cell, after stabilization, vs Room temperature.](image3)
behavior with bias conditions and temperature. Very accurate static measurements of reverse leakage current of these pnn junctions were performed using an offset compensation procedure.

The introduction of a new measurement method allowed to measure shot noise down to $3.2 \times 10^{-35} \text{A}^2/\text{Hz}$, corresponding to a current of 10 fA. In this way it was possible to determine that the actual parallel noise was larger than what expected from pure shot noise, and it was proportional to the drain-to-gate voltage ($V_{DG}$) of the input JFETs. At a temperature lower than 0 °C, the leakage current $I_{LB}$ was negligible, but a pedestal of an equivalent shot noise of 60 fA was observed for 1 V of $V_{DG}$. For 3 V of $V_{DG}$ the pedestal increased to 180 fA. The resulting series noise was very low, see table 1.

Input JFETs transistors can be operated both at room temperature and at a -6 °C to minimize parallel noise, by using a Peltier cell. A circuit was developed to stabilize the JFETs temperature. Stability was better than 50 m°C/°C, limited by the residual thermal conductance of the JFETs toward the ambient.

VIII. ACKNOWLEDGE

The intensive and invaluable technical support of Maurizio Pergo was much appreciated.

IX. REFERENCES


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<th>CMRR (In. Com. Re.) (dB)</th>
<th>Integral non linearity (%)</th>
<th>Input Offset drift voltage $\mu^\circ\text{C}$</th>
<th>Input Leakage Current(fA)</th>
<th>Eq. Shot noise 2qIEQ (fA)</th>
<th>Input series noise (nV/$\sqrt{\text{Hz}}$)</th>
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The CUORE collaboration
Reference [2]:

Room temperature differential voltage sensitive preamplifier for large mass bolometric detectors

G. Pessina*

INFN Istituto Nazionale di Fisica Nucleare, Dipartimento di Fisica dell’ Università di Milano-Bicocca, Via Celoria 16, 20133 Milano, Italy

Abstract

The present version of the very front-end preamplifier which readouts an array of 20 large mass TeO₂ bolometric detectors is reported. It operates at room temperature and has low series and parallel noise. The thermal drift has been maintained at negligible levels thanks to a correcting circuit especially designed for this purpose. © 2000 Elsevier Science B.V. All rights reserved.

1. Introduction

In the Underground Laboratory of Gran Sasso an array composed of 20 TeO₂ bolometric detectors, having a mass of 340 g each, is running [1]. The very front-end preamplifiers which readout these bolometers are differential voltage sensitive preamplifiers (DVP), designed to operate at room temperature with low series and parallel noise. The differential configuration for the signal readout allows minimizing microphonism of the connecting wires and cross-talk of adjacent channels, since both problems show up in the form of signals having common mode origin.

Large mass bolometers have a very small signal bandwidth, of a few Hz. The readout system must be DC coupled to the detector to exploit on the information contained in the signal. Any drift of the front-end is therefore a source of low-frequency noise that may impair the energy resolution.

The detector energy response is correlated with the base temperature fluctuations. One very efficient way of correcting this deficit is to correlate the detector baseline to the signal amplitude. Of course this procedure is efficient only if there is a negligible contribution coming from the front-end preamplifier.

In the following sections we will describe our preamplifier solution to the above requirements. The experimental results will also be shown.

2. The differential voltage sensitive preamplifier (DVP)

2.1. The biasing of the input JFETS

The DVP, subject of this contribution, is a simplified and more efficient new version of the preamplifier described in Ref. [2]. The circuit solution is shown in Fig. 1. The preamplifier has at the input a pair of low-noise silicon JFET, $Q_1$ and $Q_2$, biased...
to minimize their noise contribution, as described in the following.

Parallel noise is proportional to the input current of $Q_1$ and $Q_2$, which depends on the amplitude of the reverse voltage present between the gate and the channel, which forms a pn junction. A small electrical field applied to the channel minimizes the input current. This task can be obtained following two steps. By optimization of circuit design the biasing of the drain to source voltage of the JFETs, $V_{DS}$, can be chosen the minimum which assures the device to operate in saturation region, in order to obtain the right dynamic behavior. Once the drain current is fixed, the source voltage is smaller for the devices having small pinch-off voltage, $V_P$ ($V_P$ is the gate to source voltage, $V_{GS}$, for which the drain current is nulled).

The origin of the gate current, $I_{GS}$, seems largely contributed also by the effects of the intensity of the electric field applied (impact ionization) and on the doping concentration level, to which $V_P$ is proportional, in addition to the Generation Recombination, G–R current. The G–R current is proportional to the width of the depletion region [3]. It is possible to calculate its contribution by taking into account that the depletion region varies along the channel profile, when the JFET is connected to the circuit. Using the gradual channel approximation [4] and considering the device at the onset of the saturation region, after some mathematical manipulations, we have

$$I_{GS} = I_{G0} t \left( 1 - \frac{1}{6} \left( \frac{V_P}{V_{bi}} \right) \left( 1 - \frac{V_{GS}}{V_P} \right) \right).$$

In Eq. (1) $I_{G0}$ (t being the thickness of the device) is the leakage current of G–R type when the channel is totally depleted, and the source and the drain are shorted together, emulating the case of a uniform depletion set along the channel profile. The effect of the bias, drain and source at different potential, is taken into account in the term inside the brackets, where $V_{bi}$ is the intrinsic build-in voltage. From Eq. (1) it is evident that the maximum saving in G–R current is obtained when the terms inside the two round parenthesis (always $\leq 1$, consider that $V_P(0)$ are both close to unity. The saving of current obtainable in this condition is only 16%, with respect to the case in which the channel is totally depleted. Consequently, being limited by the total depletion of the channel, this current depends only slightly on any further increase of $V_{DS}$. This behavior is not observed in practice and $I_{GS}$ depends on both $V_P$ and $V_{DS}$. One practical example is given by the JFETs we have selected to fulfill our technological requirements: the pair Toshiba 2SK146, that has a pinch-off voltage having an absolute value of about 0.5 V, and the equivalent pair Inter fet IFN146 with a larger $V_P$ (0.8 V). Fig. 2 shows the measured leakage current of one of the two gates of a 2SK146 and one of the two gates of the IFN146.
as a function of $V_{DS}$, when each device pair is connected as input device of the DVP. It can be seen that both JFETs have low leakage current, somewhat larger for the IFN146 than for the 2SK146, as expected from the larger value of $V_P$. But both the leakage currents are dependent on the amplitude of $V_{DS}$, confirming a non-G–R origin for them. The comparison made in Fig. 2 is consistent, as the two devices are made with similar technological processes.

2.2. Preamplifier circuit configuration and results

The JFET input devices $Q_1$ and $Q_2$ have their $V_{DS}$ fixed to about 0.8 V thanks to the cascode connection realized with the two Operational Amplifiers, OA, OA$_A$ and OA$_B$, see Fig. 1. The reference voltage for the two OAs is taken at the virtual ground present at the common node of $R_5$ and $R_6$. The voltage drop $V_{DS}$ of the JFETs results in this way independent of the common mode input voltage. The bias current for $Q_1$ and $Q_2$ is determined for each to be about 1 mA by the current generator formed with OA$_A$ and transistor $Q_{CA1}$. Another OA, OA$_B$, is used to convert the double-ended signal at the outputs of OA$_A$ and OA$_B$ to a single ended one. The feedback of the structure is taken from the output of OA$_B$ to the source of $Q_2$. The feedback network is formed with the four resistors $R_5$ to $R_8$. The gain is given by $1 + R_6/R_8$ ($\approx 218$). The overall DC offset can be adjusted by adding suitable currents at nodes A and B. In our front-end implementation the offset is adjusted firing an automatic circuit [5].

As mentioned in the introduction, an important requirement for the preamplifier is to have a very low drift. The intrinsic drift is not small, mainly due to the JFETs. Our approach to compensate the drift was not based on the selection of temperature-matched JFETs, a very time-consuming solution, but in trying to compensate the intrinsic drift by adding in certain nodes an ad hoc current, designed for having a known thermal behavior. In the first version of our preamplifier, a proportional to absolute temperature current, PTAT current, has been derived from a commercial temperature to voltage transducer integrated circuit. In this version the PTAT current is generated from a dedicated circuit obtained from a monolithic array of low noise, matched, bipolar transistors, (CA3096M by Harris). The new solution minimizes any possible noise contribution, otherwise obtainable only by the use of very large value low pass filtering capacitances. The realized circuit is very simple and is shown in the section indicated by the horizontal bracket in Fig. 1. It is based on the fact that the base to emitter voltage of a bipolar transistor, a pn junction, is linearly dependent on temperature, with a slope of about 2 mV/$^\circ$C. Transistor $Q_{CA4}$, having the base at a fixed potential, and resistor $R_{20}$ exploit this fact and generate the thermal current $I_{TH}$, of about 400 nA/$^\circ$C. Transistor $Q_{CA2}$ and $Q_{CA3}$ generate a constant, temperature independent, current that equals the bias current of $Q_{CA4}$. As a consequence the DC current which may flow trough $R_{26}$ and $R_{27}$ has a negligible value, while the thermal current shared by the resistors is $I_{TH}$. This current is injected into the nodes A and B, the cascode nodes, which have the same potential. By proper selection of the ratio of $R_{26}$ and $R_{27}$ a thermal current, having a suitable value, can be added or subtracted from the output, correcting the original drift. The maximum DVP input drift that can be compensated in this way is about $\pm 100 \mu$V/$^\circ$C.

The selection of resistors $R_{26}$ and $R_{27}$ is made after having measured the intrinsic drift of the preamplifier inside a climatic room. So far the results obtained are very good. The intrinsic drift recorded from 45 preamplifiers, part of them having at the input the IFN146, the others the 2SK146, had an average value of 18.7 $\mu$V/$^\circ$C, with a standard deviation of 28.1 $\mu$V/$^\circ$C. After correction application, the average drift obtained on the 45 samples has become only 0.2 $\mu$V/$^\circ$C, with a standard deviation of 0.14 $\mu$V/$^\circ$C, Fig. 3. The correcting method allows therefore to reduce the drift even a factor of hundred.

The series noise of the DVP is about 30 nV/$\sqrt{\text{Hz}}$ at 0.1 Hz and 7 nV/$\sqrt{\text{Hz}}$ at 1 Hz. To save the amount of current needed for offset compensation, relatively large value feedback resistors have been used, $R_5$ and $R_6$ in Fig. 1, which limit the white noise to be about 3 nV/$\sqrt{\text{Hz}}$. This noise level does not affect the detector performance since the detector bandwidth is only a few Hz. The series noise
at low frequency is quite similar for both cases, in which the 2SK146 or IFN146 are used as input devices. The parallel noise is given by $\sqrt{2qI_G}$, and is about 0.2 fA/√Hz for the Toshiba 2SK146, becoming 0.3 fA/√Hz for the Interfet IFN146.

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### References


Reference [3]:

The Programmable Front-End System for CUORICINO, An Array of Large-Mass Bolometers

Claudio Arnaboldi, C. Bucci, J. W. Campbell, S. Capelli, A. Nucciotti, M. Pavan, G. Pessina, S. Pirro, E. Previtali, C. Rosenfeld, and M. Sisti

Abstract—We report on the front-end electronics designed for the readout of the CUORICINO experiment’s array of 60 large-mass bolometers. The front end consists of a preamplifier and a bias system for the bolometer. A significant feature of our design is its capability for in situ DC characterization of each bolometer as a function of applied bias. The principal front-end operating parameters, low-noise bias selection, load resistor selection, offset compensation, and gain are remotely programmable.

Index Terms—Detector biasing, electronics for bolometric detectors, front-end readout, high-input impedance circuit, low noise, low noise amplifier, low thermal drift, programmable system.

I. INTRODUCTION

In the case of experiments that implement an array of many detectors, accommodating the dynamic range of the detectors, demands flexibility and partial or full remote programmability in the front-end electronics [1], [2]. Bolometers, for which the manufacturing spread of dynamic characteristics is particularly broad, are especially demanding in this regard [3]. In addition, a further requirement to the readout is for very low series and parallel noise at low frequency, for both the amplification system and the bias network. Finally, a last important requirement is that the front-end drift must be negligible to allow continuous monitoring of the detector baseline.

The CUORICINO [4] experiment plans to measure an array of 60 large-mass bolometric detectors for a time exceeding two years. To limit the manual interventions in the vicinity of the bolometers during the observing period, that can interfere the measurement, we have implemented a front-end system that enables remote adjustment of the principal operating parameters, detector by detector. We begin in the next section with a system-level overview and follow in subsequent sections with descriptions of the various subsystems.

II. SYSTEM DESCRIPTION

Among the demanding constraints imposed on the CUORICINO front-end system is the restricted space into which the hardware must fit. The space available is the space now occupied by the front end [5] of the predecessor experiment MIBETA [6], an array of only 20 channels. We were thus obliged to increase the channel density by a factor of four, and we achieved this compaction while retaining standard 19 in card cages (19 in × 4 in × 10 in) as the housing for the modules.

Each card cage accommodates 15 Main Boards (MB). Each MB is 100 mm × 220 mm and comprises two complete analog channels and their associated logic circuitry. Also a very stable low-noise voltage supply/reference [7], is accommodated in every cage to service all the cards there present.

In Fig. 1, we show the functional block diagram of one of the two channels on an MB. Each channel has its own digital logic section, which sets the controls for the associated analog section. The control signals customize the analog section for the detector element that it serves. We implemented the logic section as a daughter card of the MB. The preamplifier portion of the analog section and the load resistor system are also on daughter cards.

A single input connector at the rear of the MB serves both channels. A single 37-pin “D” connector at the front accommodates the 12-lines differential analog output bus, a 10-line bidirectional digital bus, power at ±12 V and 5 V, the ±10 V supply/reference voltages, and the detector bias voltage as well as ground.

We laid out the channels symmetrically with respect to the midline of the card, and we took care in the layout to minimize crosstalk. For example the power and ground conductors are split at the midline of the module and join only at a mecca near the output connector. We measured the crosstalk from one channel to its neighbor on the MB to be at the level of −120 dB.

III. LOAD RESISTOR SYSTEM

To each element of the bolometer array is attached a Neutron Transmutation Doped (NTD) thermistor, which converts the thermal signal to a voltage signal. The bias current for the thermistor is sourced through a pair of low-noise large value thick-film 27 GΩ resistors as shown in Fig. 2. These resistors are manufactured by Siegert. They have been selected for their low 1/f noise when biased at the current levels required by the detectors [8]. $V_{16}$ and $V_{17}$ are the voltages delivered by the programmable bias attenuator described in the next section.

We represent the thermistor with a dashed line to indicate that it is within the cryostat. All other components of this circuit are at ambient temperature. We connect the cold thermistor to the warm front end with shielded twisted pair. The common mode rejection of this symmetric differential configuration effectively
suppresses adjacent-channel crosstalk and microphonic noise induced by wire vibration.

The load resistor daughter card also accommodates a pair of 6.8 GΩ resistors in surface-mount packages. By means of a bistable relay on the MB and shown in Fig. 3 we can programmably connect the 6.8 GΩ resistors in parallel with the 27 GΩ resistors for the purpose of in situ current-voltage, I-V, characterization of the thermistor. Because the relay need be energized only briefly to set its state, thanks to its memory, during normal operation it does not consume power and his coil does not create electromagnetic interference.

As shown in Fig. 3, an additional bistable relay can disconnect the preamplifier inputs from the thermistor and reconnect them to a test signal source. A test signal may be generated on the MB and inserted through the 1 MΩ resistors, or an externally generated signal may be applied directly to the preamplifier input. In the test configuration it is also possible to measure the current in the load resistors.

We adopted a number of methods in the layout to suppress parasitic conductance that might compromise the high impedance of the input nodes. First, we segregated the inverting and noninverting inputs by layer, consigning one to inner layer 1 and the other to inner layer 2. Second, we placed guard traces on the top and bottom layers paralleling the respective signal traces on inner layers 1 and 2. Third, we maintained a minimum separation of 200 mil (5.08 mm) between high-impedance pins, even at the pins of the relays. The spacing of the pins was an important consideration in the selection of the NAIS DS2ESL2-12 V for the bistable relay. Fourth, as shown in the photograph of Fig. 4, we created arc-shaped apertures in the circuit board substrate adjacent to each relay pin as a barrier to solder flux. Solder residues that elude the post-assembly wash would be problematic, but the apertures nearly eliminate the contribution of such residues to parasitic conductance. With these layout precautions and conventional industrial assembly procedures we obtain excellent results.

**IV. PROGRAMMABLE BIAS ATTENUATOR**

The inherent large spread in bolometer optimum operating point, between 100 pA and 300 pA, requires that the bias current of a channel be individually adjusted. In addition, the I-V...
bolometer characteristics are explored over a larger range, up to about 4.5 nA or 60 V across the two smaller selectable load resistors, 6.8 GΩ + 6.8 GΩ. For this reason, with each channel we include a programmable attenuator, which produces the bias voltage as an adjustable fraction of a common reference voltage. For the reference voltage source we use a single Agilent Technologies 6627A system power supply, which offers the required precision and stability.

In Fig. 5, we show the schematic of the attenuator. This circuit is an adaptation of an R-2R ladder network. The mean value of the reference inputs, \((V_+ + V_-)/2\), establishes the ground of the thermistor circuit. Then, with respect to this ground

\[
V_{\text{OUT}+} = -V_{\text{OUT}-} = \frac{n}{64} (V_+ - V_-)
\]

where \(n\) is the value of five bits of input latched in the digital section of the channel.

In the usual implementation of an R-2R ladder the upstream leads of the 2R resistors are shunted either to the reference voltage or to ground. We implement only the most significant bit, Bit1, in this manner using a bistable Double-Pole Double-Throw (DPDT) relay, for obtaining maximum accuracy. For the other four bits we adopted a less precise but space-saving strategy. The 2R resistors are permanently connected to the reference voltages through pull-up resistors \(R_p\) small compared to \(R\). For the value of \(R_p\) we selected \(R/6\). The corresponding \(R_p/2R\) junctions on the positive and negative sides of the ladder are bridged by a photo-MOS switch controlled by one of the digital input bits. When the switch is open, the \(R_p/2R\) chain increases the output voltage by an amount proportional to its position in the ladder. With the switch closed and tying the opposing \(R_p/2R\) junctions into a single node, we see that these nodes, being symmetrically placed between the positive and negative sides of the ladder, will be at ground potential as required. The use of the resistors \(R_p\) in lieu of switches is an approximation of the ideal ladder design, but it saves the scarce space that eight additional photo-MOS switches would occupy.

The 2R and R resistors in our attenuator are 560 kΩ and 270 kΩ, a ratio higher than 2:1. When the photo-MOS switch is open, the effective value of the 2R resistor is still higher, \(2R + R_p\). The maximum calculated deviation of this circuit from an ideal R-2R ladder is \(-5\%\). Measured integral nonlinearity and differential linearity with respect to each calculated setting of the implemented network of Fig. 5 was about 0.3% and 3.2%, respectively.

For the filter capacitors \(C_1\) and \(C_2\), 33 μF and 10 μF respectively, we selected parts that stand off a considerable voltage regardless of polarity. The photo-MOS switches, IR PVT 322, also stand off a considerable voltage enabling the attenuator as a whole to withstand the application of \(|V_+ - V_-| = 60\) V at its inputs.

Between the attenuator outputs and the 27 GΩ load resistors we have interposed a bistable DPDT relay shown in Fig. 3. This relay allows us to invert the polarity of the bias voltage, and by this means we can account for the thermocouple effect operating in the wires that connect the front end to the thermistor.

The noise measured between the output nodes \(V_{\text{OUT}+}\) and \(V_{\text{OUT}-}\) of Fig. 5 is 28 nV/√Hz at 1 Hz, see Fig. 6, which is negligible compared with 20 μV/√Hz, the series thermal noise of the 27 GΩ resistors.

V. THE PREAMPLIFIER

As a preliminary we offer a general discussion of four issues that substantially influence the design of the preamplifier. First, the dynamic impedance of a semiconductor bolometer is the sum of a real and a positive imaginary part [9]. For this source impedance and signals such as nuclear decays induced in the bolometer, a voltage amplifier is the conventional approach. Its performance is not superior to a current or charge configuration [10], but it allows its inputs to float. This feature makes biasing of the bolometer compatible with DC coupling.

Second, the distance from the bolometer to the front end make the input sensitive to microphonically induced noise. Our bolometers operate in the range of 10 to 100 mK whereas the first stage of the front end can operate at temperatures from a few Kelvins [11] up to room temperature. The distance separating the two thermal regimes can be no less than a few tens of centimeters and may more conveniently be a few meters. The long leads that transport the signal across the thermal gap are antennas for microphonic noise. We address this issue by making the preamplifier input differential. The amplifier noise in differential configuration is twice, in power, compared with the single-ended input, but in this case, we achieve efficient suppression of the more troublesome microphonic noise, which is predominantly common mode.

Third, for our large-mass bolometers the signal bandwidth extends from roughly 1 Hz to a few tens of Hertz. Thus, the amplifier noise, both series and parallel, must be minimized at low frequency. Finally, we must be able to monitor the baseline of each bolometer and to correlate shifts in the baseline with the bolometer’s energy gain. This capability demands adequately low thermal drift in the preamplifier.

Considering the above issues we designed and implemented the circuit shown in Fig. 7. The circuit operates at room temperature. At the core of the design is the JFET pair \(J_1\) and \(J_2\), which accepts the differential input. The series Low-Frequency (LF) noise is a major consideration in the selection of these transistors. The current source \(G_1\) [12] biases each JFET with a current of about 1 mA. We minimize parallel noise by establishing \(V_{\text{DS}}\) at about 0.8 V, the lowest value consistent with adequate gain. The op-amps \(A_1\) and \(A_2\), connected in the cascode configuration with \(J_1\) and \(J_2\), fix the \(V_{\text{DS}}\) for both JFETs to be the same as the
Fig. 5. Schematic of the programmable bias attenuator.

Fig. 6. Output noise of the BIAS attenuator system.

voltage at the top of \( R_G \). Then \( V_{DS} = I_2 R_G - (I_1 - I_2) R_S / 2 \) where \( I_1 \) and \( I_2 \) are the currents of the current sources \( G_1 \) and \( G_2 \).

The connection of the outputs of op-amps \( A_3 \) and \( A_4 \) through the resistors \( R_f \) to the sources of \( J_1 \) and \( J_2 \) closes the feedback loop. The feedback establishes the gain at \( (R_F + R_S) / R_S \), with \( R_F = 20 \, \text{k}\Omega \) and \( R_S = 91 \, \Omega \). The gain is \( 220 \, \text{V/V} \). The sources of \( J_1 \) and \( J_2 \) are directly accessible at the connectors OFF Adj + and OFF Adj – for the purpose of trimming the offset voltage. The values of capacitors \( C_1 \), \( C_2 \), and \( C_3 \), used for frequency compensation, are dependant on the op-amps adopted. The inverter \( A_3 \) enables a differential output.

Neither the input JFETs nor any of the op-amp circuits are individually compensated for ambient temperature drift. We deal with this issue by trimming the circuit as a whole. First, we operate the preamplifier in a temperature-controlled chamber to determine the untrimmed thermal response. Then, we inject at the virtual ground node labeled THERM in Fig. 7, a current proportional to temperature that will cancel the measured drift. We generate the compensating current using the circuit shown in Fig. 8. The base-collector junction of one or the other of the two transistors is the thermometer. The op-amp buffers the voltage developed across this junction, and the network \( R_A \cdot R_B \) approximately reverses the junction drop thereby allowing the op-amp output to be zero at a temperature \( T_0 \) in the vicinity of \( 20 \, ^\circ\text{C} \). The resistor \( R_{TH} \), working between the op-amp output and a virtual ground, converts the junction voltage to a current \( \Delta I = (\pm 2 \, \text{mV/}^\circ\text{C})(T - T_0) / R_{TH} \). We trim \( R_{TH} \) and set the switches \( S_1 \) and \( S_2 \) so that this current just cancels the uncompensated drift of the individual preamplifier as we measured it. The switches determine which of the two junctions is active and thus the sign of \( \Delta I / \Delta T \). With this technique we are able to reduce an uncompensated drift as large as \( 60 \, \mu\text{V/}^\circ\text{C} \) to about \( 0.1 \, \mu\text{V/}^\circ\text{C} \).

The diode used in the temperature compensation circuit should exhibit low noise, and we measured the noise of many transistors and diodes in search of a suitable device. We determined that the npn transistor BC858 is adequate for our purpose. At a bias current of \( 100 \, \mu\text{A} \) its LF noise is between \( 20 \) and \( 30 \, \text{nV/} \sqrt{\text{Hz}} \) at 1 Hz, with a \( 1 / \sqrt{f} \) slope. Taking \( V_{\text{DRIFT}} \) to be the thermal drift of the preamplifier referenced to the preamplifier input, \( V_{\text{DRIFT}} \) to be the temperature coefficient of the BC858 junction, roughly \( -2 \, \text{mV/}^\circ\text{C} \), \( A \) to be the voltage gain, \( 220 \, \text{V/V} \), and \( \alpha \approx R_3 / R_{TH} \), where \( R_3 \) is from Fig. 7 and \( R_A \gg R_B \) in Fig. 8, we see that we achieve compensation provided that \( \alpha V_{\text{DRIFT}} = A V_{\text{DRIFT}} \). With \( c_{DN} \) representing the junction noise, the contribution of the temperature compensation circuit to the noise budget, referenced to the input is

\[
\frac{c_{\text{DN}}^2}{c_{\text{IN}}^2} = \left( \frac{V_{\text{DRIFT}}}{V_{\text{DRIFT}} + V_{\text{DD}}} \right)^2 \frac{c_{\text{DN}}^2}{c_{\text{IN}}^2}.
\]

For example, for a large initial drift of \( 60 \, \mu\text{V/}^\circ\text{C} \) and \( 30 \, \text{nV/} \sqrt{\text{Hz}} \) diode noise, temperature compensation will contribute \( 0.9 \, \text{nV/} \sqrt{\text{Hz}} \) at 1 Hz, which is to be added in quadrature with the preamplifier noise.

The noise level of this preamplifier is quite suitable for the application. The gate current of each JFET is less than \( 0.3 \, \text{pA} \), which corresponds to parallel noise of about \( 0.3 \, \text{fA/} \sqrt{\text{Hz}} \). The series noise of the preamplifier, after temperature compensation, is shown in Fig. 9. The LF noise is about \( 4.6 \, \text{nV/} \sqrt{\text{Hz}} \) at 1 Hz with a \( 1 / \sqrt{f} \) slope. The white component, \( 2.5 \, \text{nV/} \sqrt{\text{Hz}} \), arises in roughly equal parts from the JFETs and the thermal noise of the \( 91 \, \Omega \) feedback resistors \( R_S \). Making these resistors smaller would reduce the noise, but then the offset voltage trim currents (at the OFF Adj + and OFF Adj – nodes of Fig. 7) would become unacceptably high. Much of the offset voltage results...
VI. THE OFFSET CORRECTOR

Because the bolometer is DC coupled to the front end, the biasing contributes to the input offset voltage. In this situation a sophisticated system for offset trimming is more than a convenience. As low noise is a prerequisite in our application, the offset corrector and its reference source clearly must also conform to the low-noise criterion.

For the voltage reference we adopted a design that we described in an earlier report [7]. This solution avoids a local monolithic reference and its extremely low-pass filter, by implementing them in the unit that supply the circuit with the +10 and −10 V voltage. The reference voltages used in the offset corrector, −2.12 and +6.76 V, are derived locally from the system-wide references using resistive dividers.

The application of a differential current $\Delta I_{\text{CURR}}$ through the preamplifier connections OFF Adj + and OFF Adj − to the JFET source resistors $R_S$ (see Fig. 7) will generate the offset compensating voltage $V_{\text{OFFSET}}$. Clearly

$$\Delta I_{\text{CURR}} = \frac{V_{\text{OFFSET}}}{R_S}. \quad (3)$$

The bolometer bias voltage is typically between 10 and 20 mV. For characterizing DC behavior, however, a bias voltage as high as 50 mV may be appropriate. The JFETs can contribute an additional ±20 mV to the offset budget. A range for $V_{\text{OFFSET}}$ of ±80 mV is thus conservative, and with $R_S$ set at 91 Ω (3) gives a corresponding range for $\Delta I_{\text{CURR}}$ of about 900 μA.

The correction current $\Delta I_{\text{CURR}}$ is the difference $I_{\text{off+}} - I_{\text{off−}}$ where these currents appear at the outputs of the pair of current sources shown in Fig. 10. The resistor chain $R_{\text{EF}} - R_3$ sinks only 35 μA and allows both current sources to remain conducting regardless of the state of the switches. A current with the magnitude of $\Delta I_{\text{CURR}}$ flows from node A through one current source.
or the other depending on which one of the switches Sign- and Sign+ is closed. For the switches we use the MAX4605, which is a MOS switch with a low resistance, $R_{on} = 5 \ \Omega$. The resistors $R_1, 1 \ \text{k} \Omega$, load the outputs of the op-amps and so improve their stability. The op-amps ensure that the MOSFET source voltage is the same as the reference, $-2.12 \ \text{V}$. The MOSFET drains are in common with the sources of the JFETs of the preamplifier circuit (Fig. 7), and these are generally at a positive potential because in normal operation the common-mode voltage appearing at the preamplifier inputs is close to $0 \ \text{V}$.

Our objective is that the current inserted at node A of Fig. 10 should be programmable, and thus we need to incorporate a digital-to-analog converter, a DAC, into our design. A commercial DAC would be convenient, but generally the output buffer of these devices renders them excessively noisy for this application, particularly for DAC based on CMOS technology. The DAC that we adopted, the 12-bit DAC8043A, circumvents this problem by omitting the output buffer, and it is not enough for the noise performance needed. The DAC adopts operate by means of a current scaling R-2R network. Unfortunately resistors on integrated circuits exhibit LF noise proportional to the square of the applied voltage [13], [14]. Fig. 11 shows the noise from the DAC8043A with three choices of the reference voltage and confirms the last assertion. The noise from this DAC is tolerable provided the reference voltage is sufficiently low, but then the maximum current derivable from it is inadequate. Our solution was to cascade the DAC8043A with an external low-noise buffer amplifier, implementing a small precise and low noise trimming of the offset at the front-end output. The additional increase of the needed correction range has been obtained by injecting to the node A of Fig. 10 a correcting current provided by two low noise resistors, digitally controlled by switches. The DAC buffer can generate only a quarter of the maximum correcting current, the remaining being given by the two digitally selectable resistors.

Fig. 12 shows this solution. The metal-film resistors R and 2R, which set the supplemental current, introduce negligible LF noise. With value $18 \ \text{k} \Omega$, R enables the movement of $V_{OFFSET}$ by $40 \ \text{mV}$, and 2R enables an additional $20 \ \text{mV}$. With $V_{REF}$ at $6.76 \ \text{V}$ the DAC8043A contribution to the noise is only $0.9 \ \text{nV/} \sqrt{\text{Hz}}$ at $1 \ \text{Hz}$ referred to the preamplifier input. Working through $R_{DAC}$, $30 \ \text{k} \Omega$, the DAC8043A can move $V_{OFFSET}$ by $20 \ \text{mV}$, bringing the total excursion available to the desired $80 \ \text{mV}$.

The resistor $R_{0V}, 120 \ \text{k} \Omega$, sinks the current that would otherwise flow through $R_{DAC}$ into A even when the DAC8043A output is at $0 \ \text{V}$. Because resistors R and 2R have a precision of 1%, some narrow gaps may exist in the accessible range for $V_{OFFSET}$. These gaps have been partially taken into account by the addition of overlapping codes within the DAC range. The op-amp $A_1$, an LT1881, contributes to the noise at the level of $0.55 \ \text{nV/} \sqrt{\text{Hz}}$ at $1 \ \text{Hz}$. The noise from the $-10 \ \text{V}$ reference is about $95 \ \text{nV/} \sqrt{\text{Hz}}$ at $1 \ \text{Hz}$ and in the worst case may contribute $0.94 \ \text{nV/} \sqrt{\text{Hz}}$ at $1 \ \text{Hz}$ referred to the preamplifier input.

In Fig. 13 we show our measurement of front-end noise when the maximum offset compensation current is injected into the preamplifier. Comparing Fig. 13 with Fig. 9, we conclude that the increment of the compensation circuit to the noise of the preamplifier alone is at worst 4% at $1 \ \text{Hz}$ and becomes negligible at higher frequencies.

Under the control of the digital section a channel may autonomously trim its offset using a successive approximation method. Initiation of this process is by command delivered on the digital bus or by activation of a button on the MB front panel. The digital board determines the state of the bit under test by reading the output of the discriminator shown in Fig. 1. The comparator has a threshold of $114 \ \text{mV}$ and a hysteresis of $32 \ \text{mV}$. The algorithm requires one cycle to set the polarity switches (Fig. 10) as well as a cycle for each of the 14 magnitude bits.
Allowing this algorithm to run too fast may have two adverse consequences. First, inadequate settling times may introduce errors. Second, the system, acting like a unity-gain feedback loop, may break into oscillation. Slowing down the process solves both problems. The offset corrector algorithm operate with a reduced clock obtained from the output of a programmable counter.

After a channel has trimmed its offset, the resulting value of the DAC code is available via the bidirectional digital bus. Any value of offset may then be established by suitably adjusting this code and sending the new code to the channel. The Special bit, S-bit, shown in Fig. 12, facilitates such manipulations of the offset voltage. The current that it controls corresponds to roughly half of the range of the DAC8043A. If the code corresponding to null offset is in the lowermost quarter or the uppermost quarter of the DAC8043A range, then setting the S-bit and retrimming will shift the code for null offset to a value in the middle half of the range. For one setting of the S-bit or the other an excursion of the offset voltage by at least a quarter the range in both directions is possible without alteration to the less precise high-order bits 12 and 13. A quarter of the DAC8043A range corresponds to 5 mV at the input and a minimum of 1.1 V at the output. This range of correction is largely able to comply with the dynamic range required by the application.

VII. THE PROGRAMMABLE AMPLIFIER AND SYSTEM NOISE PERFORMANCE

The final stage of the signal processing chain is the programmable gain amplifier, which we show in Fig. 14. The circuit provides a digitally selectable choice of 32 values of gain in the range from 220 to 5000 V/V from preamplifier input to module output. Both input and output are differential. In this circuit we use metal-film resistors, MAX4605 switches, and AD822 op-amps. These components all have adequate LF noise behavior.

Because bolometers spread their characteristics over a large range, it is difficult to estimate the noise figure of the implemented readout. We try to do this considering the mean energy resolution of 3.1 keV$_{FWHM}$ obtained from MIBETA experiment [4], with the best performance of the array close to 1.8 keV$_{FWHM}$. This performance is expected to be maintained also for CUORICINO [15], that foreseen bolometers with a mass as twice as those of MIBETA. The above mean resolution is obtained when the bolometer dynamic impedance is about 20 MΩ, the noise is about 0.82 nV$_{FWHM}$, and the frequency bandwidth of the signal is about 10 Hz [4]. The noise of the whole analog system, both series (about 6 nV/√Hz at 1 Hz, 1/f slope) and parallel (about 0.4 fA/√Hz), results in about 37 nV$_{FWHM}$. The parallel thermal noise of the 2 × 27 GΩ load resistors is 82 nV$_{FWHM}$. Load resistors 1/f noise is negligible at the typical bolometer bias level of about 150 pA [4]. The total contribution results in about 90 nV$_{FWHM}$, dominated by the load resistors. This is considerably smaller than the noise quoted above, even for the better bolometers of MIBETA, proving that the designed front-end is adequate for this experiment.

VIII. THE DIGITAL CONTROL BOARD

The Digital Control Board (DCB), communicates via a 10-bit bidirectional bus [6] with a personal computer. The low-order eight bits carry the data, and the high-order two bits carry the instruction code. Each channel in the system has a unique address, and the computer communicates with one channel at a time. The rudimentary protocol proceeds through four steps: addressing the channel, sending the command, transferring the data, and closing the transaction.

An RC oscillator built around an NE555 timer chip furnishes a 3.9 kHz clock to the DCB. The comparatively low frequency allows error-free communication even if the bus must be rather long. Because electrical noise originating from the clock is undesirable during data acquisition, the DCB can shut down the oscillator and normally allows the clock to run only when needed.

Each channel includes one Complex Programmable Logic Device (CPLD) for the implementation of the DCB functions. In addition the two channels on a MB share a third CPLD, which manages the communication. All three CPLDs are the Xilinx XCR3128XL. An uncommon feature of this device is that its outputs can remain active even when the clock is idle. A second feature that suits the XCR3128XL to our application is the low current consumption, only a few microamps at the operating frequency.

Signals exchanged between any channel and the computer pass through digital opto-couplers, which facilitates isolation of...
the front-end ground from the computer ground. This isolation helps to protect the front end from disturbances in the computer ground.

IX. Conclusion

We have designed front-end electronics that meet the stringent requirements of the CUORICINO bolometric detector. The principal sections of this front-end are an extra low-noise differential preamplifier, a second stage amplifier with programmable gain, a programmable system for setting the thermistor bias, and a programmable system for setting or nulling the input offset voltage. The remote control capabilities minimizes the need for disruptive physical activity near the detector during data acquisition. We have fabricated the 60 channels that the experiment requires. Two standard 19 in card cages are sufficient to accommodate all of these channels.

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Reference [4]:

The front-end readout for CUORICINO, an array of macro-bolometers and MIBETA, an array of $\mu$-bolometers

C. Arnaboldi$^a$, C. Buccib, S. Capellia, A. Fascilla$^{a,c}$, P. Gorlab, A. Nucciottia, M. Pedrettia,c, G. Pessina$^{a,*}$, S. Pirro$^{a,b}$, E. Previtalia, M. Sistia

$^a$INFN—Istituto Nazionale di Fisica Nucleare and Dipartimento di Fisica della Bicocca, P.za della Scienza 3, Milano 20126, Italy

$^b$INFN Laboratori del Gran Sasso, Strada Statale 17bis, Km 18+910, 67010 Assergi (AQ.), Italy

$^c$Universita dell’Insubria, Facoltà di Scienze CC FF MM, Via Valleggio 11, Como 22100, Italy

Abstract

The front-end approach for the readout of two arrays of bolometric detectors is described. The first front-end is for an array of $\mu$-bolometers, while the second is for an array of macro-bolometers. Analogies and differences in the adopted strategies are put into evidence.

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Keywords: Front-end; Low noise; Amplifier; Cryogenic detectors

1. The front-end of MIBETA

MIBETA and CUORICINO are two arrays of bolometers. The MIBETA array is composed of 10 very small mass detectors, or $\mu$-bolometers, each 260 $\mu$g on average. CUORICINO, by contrast, contains 62 channels and is the prototype of an array consisting of very large mass detectors, 760 g each. The MIBETA experiment, just stopped, was realized to study the electron anti-neutrino mass in the $\beta$ decay of $^{187}$Re [1]. The main system requirements for this experiment were good energy resolution and fast detector speed. We met both conditions by utilizing bolometers of small mass.

The dynamic impedance of a bolometer has both resistive and inductive components. To obtain high speed, 5–10 kHz bandwidth, the front-end input capacitance must be very small, to minimize signal integration.

In Fig. 1, we show the schematic diagram of the front-end of every channel of the MIBETA array. The bolometer, with impedance $Z_B$, is operated at about 90 mK, while its load resistor, $R_L$ (1 G$\Omega$), is held at about 20 mK. The signal is readout, through a short, high impedance link, using a Si JFET ($Q_1$), which works at its optimum temperature of about 110 K in a source–follower configuration. A room temperature differential voltage preamplifier (1000 V/V gain), PA, subtracts from the signal at the source of $Q_1$ any common mode disturbance present at the ground lead of the bolometer. A programmable amplifier (2–26 V/V...
noise is totally negligible, since the vanishing value due to the low-frequency contribution. Parallel frequency component leads it to $2 \text{nV} = 4 \text{nV}$ at 1 Hz. The cold JFET has a white voltage noise of the input of PA is about 1 nV if not rejected.

The undershoot would be seen as a spurious signal if the trigger circuit is AC coupled, the rising edge of the coupling of the inductive component of the bolometric impedance with the shunting capacitance of the connecting link. Since the boltomator, Z_B, which is operated at about 10 mK. The link that connects Z_B to Q_1 and Q_2 is a twisted cable that minimizes signal cross-talk, microphonics of the link itself, and electromagnetic interference.

The differential voltage preamplifier, PAC, (220 V/V gain) reads the signal at the sources of the gate current. The cold JFETs are biased to minimize their power consumption: $V_{DS} = 1 \text{V}, I_{DS} \approx 0.3 \text{mA}$. The present version of the cold front-end gives a negligible contribution to the energy resolution when the array is operated at 60 mK, where the signal-to-noise ratio is a maximum. At the chosen operating condition of 90 mK, a trade-off between high speed and adequate energy resolution, the detector noise lower and the front-end noise rises its contribution to a factor of about $\sqrt{2}$.

2. The front-end of CUORICINO

The aim of CUORICINO is to study the neutrinoless double $\beta$ decay of $^{130}\text{Te}$ [2]. Each detector of the array is composed of a 760 g TeO$_2$ crystal to which a Ge NTD thermistor is glued.

The very slow signal bandwidth is the main feature of a massive bolometer. For CUORICINO it is 8 Hz, on average. As a consequence, the front-end electronics must contribute very little noise at small frequencies. It must also has very little drift, since the readout must be DC coupled to the detector.

As a result we have adopted the strategy shown in Fig. 2. A differential, cold, buffer stage that works at about 100 K, is located closed to the bolometer, $Z_B$, which is operated at about 10 mK. The load resistors $R_L$ (each 27 GΩ) are located near the buffer stage, at 100 K. The link that connects $Z_B$ to $Q_1$ and $Q_2$ is a twisted cable that minimizes signal cross-talk, microphonics of the link itself, and electromagnetic interference.

The differential voltage preamplifier, PAC, (220 V/V gain) reads the signal at the sources of the macro-bolometers CUORICINO.
$Q_1$ and $Q_2$. The second stage PGA and PGF are similar to the ones described in the previous section, except the range of the gain, 1–45 V/V, and the filtering bandwidth, 8–20 Hz with 6 poles of roll-off. Since the frequency bandwidth is small, and the roll-off of the filter is steep, it was not necessary to use a linear buffer optocoupler to suppress GL.

The current source POA auto-adjusts the output offset. The trigger circuit TRS is an AC coupled (2–10 V/V gain) amplifier with the same re-triggering suppression circuit as for MIBETA.

The cold stage for CUORICINO has been used to read-out 24 detector channels. Two metallic boxes, anchored at the 4.2 K plate of the refrigerator, each contain two boards with 6 differential buffer channels and the load resistor pair. The remaining 38 channels of the array do not make use of the cold buffer stage, $Q_1$ and $Q_2$ of Fig. 2, and the detectors are directly connected with a twisted cable to the preamplifier PAC. In this case the load resistors ($R_L$, each 27 GΩ) are at room temperature. An additional bus, AUX, can be connected to any output channel independently from the DAQ. This bus is used for the DC characterization of the bolometers and monitoring.

The cold buffer stage has the JFET operated at $V_{DS} = 0.5$ V and $I_{DS} = 0.3$ mA. The resulting voltage noise is about 10 $\text{nV}/\sqrt{\text{Hz}}$ at 1 Hz, while 2 $\text{nV}/\sqrt{\text{Hz}}$ is its white term. Current noise is totally negligible. The voltage noise of PAC is 4 $\text{nV}/\sqrt{\text{Hz}}$ at 1 Hz; 3 $\text{nV}/\sqrt{\text{Hz}}$ white. The current noise is about 4 $\text{fA}/\sqrt{\text{Hz}}$. A special circuit has been introduced in PAC that allows reducing the input drift to $\leq 0.2 \mu\text{V}/\text{C}$. The electronics circuit described above adds negligible noise to the CUORICINO array.

The programmability of all the described features, for both MIBETA and CUORICINO, can be set remotely, via a fiber-optical link.

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Letter to the Editor

A self-buffered DC baseline restorer with quasi-ideal behavior

Cesare Liguori, Gianluigi Pessina

AEDI, Strumenti Scientifici, Via A. De Gasperi 19, 20020 Lainate, Milan, Italy
INFN, Istituto Nazionale di Fisica Nucleare and Dipartimento di Fisica, dell'Università, Via Celoria 16, 20133 Milano, Italy

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Abstract

We present a DC baseline restorer featuring quasi-ideal behavior, capable of showing an undershoot of less than 0.023%. Its circuit structure allows using a single operational amplifier to realize both the buffering of the output signal, with line driving capability, and to discharge the decoupling capacitance. The operational amplifier in each working condition always remains in a closed-loop state, exploiting its full dynamic performance. The presented circuit allows the avoidance of an additional amplifying buffer stage, necessary, up to now, to drive a 50 Ω coaxial cable terminated at both ends.

Keywords: DC baseline restorer; Circuit

1. Introduction

Applications with large number of acquisition channel need front-end systems having low-cost and reduced space occupation. To this aim we have studied and realized a DC Baseline Restorer (BLR) which, despite the minimum number of electronic components, shows outstanding performance. The BLR subject of this letter is a circuit solution for the classical configurations described in Refs. [1,2] and analyzed in Ref. [3]; our circuit is a feedback structure always operating in closed-loop condition, and incorporates line driving capability. In this way, a complete spectroscopy amplifier composed of an adjustable two-gain stage, a RC-CR shaper and a BLR can be easily implemented with a single quad operational amplifier chip.

The following section describes in detail the complete BLR circuit and the experimental results.

2. Principle of operation of the DC baseline restorer

The front-end of a nuclear detector includes at the end of the chain a shaping filter and a post-amplifier. AC coupling is usually adopted to avoid the presence of undesirable DC offset, which may impair the actual final resolution, when a high rate of events is present. The drawback of such a coupling is the undershoot given by the decoupling capacitance, which cannot transmit a net amount of energy. This problem is solved using the BLR, which, in essence, is a high pass single pole filter whose time constant varies depending on the signal state. Assuming positive signals, when the output is
in its negative state the BLR must be able to discharge the decoupling capacitance with a negligible time constant. This is usually obtained by connecting an active impedance of negligible value at the output terminal of the capacitance, implemented with diodes which switch ON or OFF, when necessary.

3. The self-buffered DC baseline restorer

The BLR is a classical circuit that has been implemented in many different ways, [4–9], even with the current conveyor technique [10]. Nevertheless, up to now the circuit solutions are all active only when in the discharging state, while they behave as passive networks in the signal transmission state. The consequence is that a buffering of the signals is always necessary for driving the output, especially when a terminated line has to be fed. In addition, since the circuit must translate from the transmission to the discharging condition, distortions may be present if the system gain is large.

In the presented solution a circuit has been implemented which uses a single Operational Amplifier, OA, that is operative in both states, discharging and transmission. This way a number of advantages have been obtained. In the discharging state the large open-loop gain of the OA allows the implementation of an ideal short-circuit for the capacitance discharge. No effects are seen at the output when the network translates from the discharging to the transmission state, thanks to the fact that the OA is operating always in linear regime. Since the OA behaves as a buffer in all conditions, the output is able to drive directly a 50 Ω coaxial cable terminated at both ends: the circuit is self buffered. The self-buffered BLR circuit is of very simple implementation and has a very low cost, since it needs only a few components.

The circuit solution is shown in Fig. 1. When in the transmission state, the new BLR behaves as a unity gain inverting amplifier. The input signal is connected at the decoupling capacitance $C_C$. If the signal is falling fast enough, in comparison to the time constant $C_CR$, inducing the output to become positive, $Q_1$ is able to feed the load impedance present at its emitter, while the Schottky diode $D_1$ remains in the OFF state. The network behaves simply as a unity gain buffer amplifier (gain – 1) since resistors $R$'s are equal (resistor $R/2$ only compensates the OA’s input bias current). We can take advantage of this condition for buffering the signal on a transmission line. If now the input signal becomes rising or slows down, such that the output should become negative, $Q_1$ is no longer able to feed the load, going in its OFF state. But since the OA has a large gain, as soon as its inverting input tends to lower the OA output, $D_1$ enters its conducting condition, maintaining the OA in the closed-loop state and promptly discharging capacitance $C_C$. While in this working condition, the output voltage $V_{OUT}$ is zero, since the inverting input remains at zero volts and $Q_1$ is OFF: signal current flow into resistors $R$ is zero. As a consequence, the potential at the anode of $D_1$ is the same as that present at the inverting input: $C_C$ is then discharged to ground. This way we have achieved the simultaneous conditions that the output never becomes negative and the capacitance $C_C$ is connected to an active load that has an ideally negligible impedance when in the discharging state.

The circuit of Fig. 1 has been tested experimentally. The OA used was the monolithic EL2044, which features large bandwidth and high slew rate, to assure good linearity up to 10 V of output signal. The capacitance $C_C$ is 10 nF. The oscilloscope plot of Fig. 2 shows the circuit response to a train of semi-Gaussian impulses of 1 μs time constant, read from an Ortec 450 spectroscopy amplifier. The output signal was sent to the two inputs of the oscilloscope, and terminated with 50 Ω at both ends of the connecting coaxial cable. On one scope input the signal is shown full scale, while it is zoomed on the other input, to document the
4. Conclusions

A new self-buffered DC baseline restorer has been implemented. Its main feature is based on the use of a single Operation Amplifier, OA, which always works in its linear region, with a double feedback loop, one for the buffering of the signal, the other for the discharging of the decoupling capacitance. Taking advantage of the large open loop gain of the OA, an ideal active impedance of negligible value is obtained for the discharging of the capacitance. On the other side, the buffering of the signal allows direct driving of terminated 50 Ω coaxial cables, saving the use of an additional circuit devoted to this purpose, as needed in previous solutions. The measured undershoot following the signal was practically negligible, being less than 0.023%, proving that a quasi-ideal behavior has been obtained.

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Reference [11]:

A very simple baseline restorer for nuclear applications

Claudio Arnaboldi*, Gianluigi Pessina

INFN Istituto Nazionale di Fisica Nucleare and Facoltà di Fisica dell’Università della Bicocca, Piazza della Scienza 3, Milano 20126, Italy

Abstract

We present a series of Baseline Restorer circuits (BLR) all based on a very simple and compact configuration. The circuits are able to withstand signals shaped as fast as 10 ns or as slow as hundreds of ms. These BLRs are improved versions of an already existing solution that has shown outstanding performances. We have now introduced new features to the original configuration capable of improving the operation of the stationary condition of the stage that precedes the BLR output. This way the response of the circuit to the incoming signal is further improved. In addition, special attention has been paid to obtain large speed of response. Signal rates as large as 10 MHz with large pile-up percentage are easily supported. This property is particularly suitable for the next generation of experiments at the large hadron colliders at CERN. One version of the described BLRs is presently used in the analog section of the trigger system of the experiment CUORICINO, an array consisting of 70 large mass bolometric detectors. For this experiment, the BLR is capable of guaranteeing a very precise baseline that allows to trigger very small signals for the Dark Matter study. Typical shaping times for this kind of bolometric signal are in the tens to hundreds of milliseconds range. The addition of a further simple circuit solution has permitted to suppress the problem of the re-trigger error coming from those large signals that present an undershoot, due to a non-perfect return-to-zero of the bolometric signals. Although having a different origin, this phenomenon can be thought as equivalent to a non-perfect pole-zero cancellation. The complete circuit diagrams of the BLR will be shown and the experimental results will be addressed in detail.

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Keywords: Baseline restorer; Nuclear electronics; High-speed circuit

1. Introduction

In a nuclear acquisition chain an AC coupling is very often made between the front-end and the ADC, Fig. 1. If the pulse rate is large and the shaping time filter used is not bipolar the DC component of the signal is shifted to zero at the input of the ADC. The shift comes from the capacitance $C_A$ that does not allow the DC components of the signals to feed the ADC. If $\bar{V}_d$ is the average amplitude of the signal pulses at the output of the shaper of Fig. 1, $A_R$ is the area of the pulse having unity amplitude and $\nu$ is the average rate, then the average or DC component of the signal is

$$V_{DC} = \nu A_R \bar{V}_d$$

The above equation is known as Campbell theorem. The voltage $V_{DC}$ varies instant by instant, so measurement errors are made if this effect is not taken into account or suppressed.

To obtain both AC coupling and avoid the baseline shift a non-linear circuit is adopted, the
so-called Baseline Restorer (BLR). In essence, the BLR is a system that has a response that is correlated with the sign of the slope of the signal. One of the simplest ways to look at it is as in Fig. 2, where the simplified schematic diagram of the solution by Robinson [1,2] is shown. In the circuit of Fig. 2 the rising edge of the signal injects a current in $C_A$ that increases the voltage at node $V_0$, increasing the dynamic resistance of diode $D_1$, while the falling edge of the signal develops a current in $C_A$ that tries to lower the potential of the same node, lowering the dynamic resistance of $D_1$. The result is that the coupling time constant is large for the rising part of the signal, and becomes very small for the falling part of it. Capacitance $C_A$ is charged and discharged in an asymmetric way, avoiding the baseline shift effect, that comes about from the balance of the positive and negative derivative of the signal. The circuit of Fig. 2 has as a drawback the imprecision that comes from the dropout dependence of the diode voltage with the current flow.

Many circuit solutions exist that try to minimize the diode dropout effect [3–10]. Every readout solution presents a residual undershoot in the response that depends on the circuit efficiency. We have already developed a BLR, showing quasi-ideal performances [12], based on an improved version of the Gere–Miller restorer [3]. In the following sections, we will show in detail new features added to our solution that allow improving even more the BLR performances, and enabling it to operate at very large counting rates. On the other hand, the circuit is very suitable also for applications where the speed of response is very slow, but a high precision is required. As an example the described BLR is used to generate the analog trigger for each of the 70 bolometers that compose CUORICINO, an array of large mass cryogenic detectors [11]. In this application the frequency bandwidth of signals is only a few Hz. An additional very simple circuit solution has been further added to the BLR to cancel the re-trigger effect from those large incoming signals that present undershoot.

1.1. An ideal baseline restorer

The concept of the BLR we have developed [12] is very simple, Fig. 3. Let us suppose that the incoming detector pulse has negative polarity. On the falling edge of the signal the current comes from the emitter of transistor $Q_1$, following the direction indicated by $I_F$:

$$V_0 = -\frac{R_B}{R_A} \frac{sC_A R_A}{1 + sC_A R_A}.$$ (2)

When the input pulse rises and the current through $C_A$ inverts its direction, then the output crosses the zero voltage level. After this condition is met the current will follow the path indicated by $I_R$. In this case diode $D_1$ will become forward.
biased discharging capacitance $C_A$ promptly. Since the Operational Amplifier (OA) is in closed-loop condition node A results as a virtual ground and the output can only be at zero potential since transistor Q1 cuts off. In addition, the feedback makes the dynamic resistance of D1 negligible, so $C_A$ is therefore discharged by an ideal virtual switch. No particular requirements are imposed on the time constant $R_A C_A$ in comparison to the pulse width, as will be evident in the results shown below.

So far we have shown that the OA works in closed loop in both working conditions. In addition, the OA itself behaves also as a buffer amplifier. The feedback action of the circuit solution adopted allows the equivalent impedance of both transistor Q1 and diode D1 to appear very small while forward biased, very large otherwise. With respect to the Gere–Miller restorer circuit we add transistor Q1 that maintains the OA always in closed-loop condition, improving much the speed of response. In addition, the voltage across $C_A$ is now buffered. It has to be remarked that all these features are obtained using only one amplifier that serves all the operations needed.

We introduce now a number of different improvements to the circuit of Fig. 3 that make our BLR very close to the ideal behavior.

From the above description the working condition of the circuit is known when the signal is present. Although the output of the system remains zero when there is no signal present, the equilibrium condition at the output of OA, node B of Fig. 3, is not established and may oscillate between the two states at $+V_{BE1}$ or $-V_{D1}$ ($\approx \pm 0.6$ V). To avoid this effect one solution is illustrated in Fig. 4. Resistors $R_{F1}$ and $R_{F2}$ set a DC path between the inverting input and the output node of the OA. This path is broken at large frequency by the presence of the filtering capacitance $C_F$. In this case the circuit has its output at the middle voltage between the two working conditions, $+V_{BE1}$ or $-V_{D1}$, ready to start. When a large resistor, $R_F$, can be used, a solution that allows saving one resistor and capacitance $C_F$ is shown in Fig. 5.

1.2. Application of the BLR to bolometers

In case capacitance $C_A$ is large and the OA output has a limited current sinking capability, the configuration of Fig. 5 can be modified as in Fig. 6. The principle of operation remains exactly the same, but now the discharging of $C_A$ is through the pnp transistor Q2 rather than through a diode and the OA output now drives only the base current of the transistor.

This is the case with bolometers where the AC coupling frequency is a few Hz and $C_A$ is very small.
large, about 50 μF. The combination of diode D₁ and resistors R₁ guarantees that the equilibrium voltages V_B, at the OA output, and V_C, at the base of Q₂, are half a diode voltage drop, V_B ≈ V_{BE}/2 and V_C ≈ −V_{BE}/2. This condition assures that Q₁ and Q₂ are biased in sub-threshold region in the waiting state, and the change to any operating conditions needs a reduced step voltage at the OA output to put either one forward biased. Sometimes a diode is needed in series with the base of Q₂ to avoid breakdown of the base to emitter junction if large reverse bias excursions are expected.

Large mass bolometers generates signals whose frequency bandwidth is extremely small, a few Hz. In addition, they show a dynamic impedance that has an inductive component. If shunted with a parasitic capacitance the generated signal may have a small undershoot. If the trigger threshold must be very small, the AC coupling of the trigger circuit can re-trigger on the rising part of the undershoot for those signals that have a large amplitude. To avoid the re-trigger effect we have added the network R_C, C_C to the BLR of Fig. 6, obtaining the solution shown in Fig. 7.

The principle of operation, on a qualitative basis, is as follows. Let us suppose that τ_C = R_C C_C ≫ τ_A = R_A C_A and consider the undershoot of the signal as an exponential decay, \( v_{i0} \exp(-t/\tau_T) \). The current trough \( R_A \), \( C_A \), \( I_A \), is the quasi-derivative of the undershoot, or about:

\[
I_A \approx -\frac{1}{R_A} \frac{\tau_A}{\tau_T} v_{i0} \exp(-t/\tau_T)
\]

while the current trough \( R_C \), \( C_C \), \( I_C \), is simply proportional to the undershoot:

\[
I_C \approx \frac{1}{R_C} v_{i0} \exp(-t/\tau_T)
\]

The two currents are opposite and cancel out when it is satisfied:

\[
\frac{R_A}{R_E} \approx \frac{\tau_A}{\tau_T}
\]

By making the same calculation in the frequency domain, we get \( s = j\omega \)

\[
i_A(s) + i_C(s) \approx \frac{s}{R_A} \left( s + \frac{1}{\tau_A} \right) \left( s + \frac{1}{\tau_C} \right) v_i(s).
\]

In the above equation, it has been assumed that \( \tau_C \gg \tau_A, \tau_T \) and Eq. 5 is satisfied.

The \( R_C \), \( C_C \) network adds a zero that can be chosen to cancel the pole \( \tau_T \) eventually present in the input signal \( v_i \). The cancelled pole is substituted by a new pole, \( \tau_C \), of much larger values that broadened the undershoot over a much larger interval of time, attenuating its amplitude strongly. The experimental result of the efficiency is given in the scope pictures of Fig. 8. In Fig. 8a, a typical bolometric signal having an undershoot of about 10% is simulated with an arbitrary function generator, Agilent 33250A and sent to the BLR input. The signal has a negative polarity and it is inverted at the scope screen to guide the eyes. The amplitude is about 5 V. On the same photograph the BLR response to the signal is zoomed when the pole-zero compensation is not present. As can be seen in Fig. 8a once the undershoot of the input, which roll off with a time constant of about 4 s, gets a positive slope the BLR output generates a signal that may give a wrong trigger. In Fig. 8b, the same simulated signal is instead input to the BLR when the \( R_C \), \( C_C \) network is set properly to cancel for the undershoot. As can be seen the effect of the re-trigger is almost eliminated.

1.3. BLR with fast signals

The BLR realized like all the others must change the state of operation of a non-linear device, a diode or a transistor, when fired by a signal. This action may limit the speed of response of the
Let us refer to the BLR of Fig. 4 and suppose it in equilibrium with node B close to 0V. If a signal is now applied the output will follow the input only after the time necessary for the OA to switch transistor $Q_1$ into operation. Consequently, some information is lost in the first part of the signal. We can try to estimate this time interval.

Let us suppose the OA transfer function approximated with a dominant pole behaviour and consider the gain at DC very large. The output of the OA, node B, is

$$V_B(s) \approx \frac{\omega_A}{s} v_i(s)$$  \hspace{1cm} (7)

where $\omega_A$ is the unity gain frequency of the OA. In the time domain Eq. (7) is the integral of $v_i(t)$. For the case $v_i(t)$ is the output of a RC-CR shaping time filter with time constant $\tau$, the integration is quite simple and, for small time, results in

$$V_B(t) \approx \frac{\omega_A}{\tau} v_i_0 t^2$$  \hspace{1cm} (8)

where $v_i_0 \exp(-1)$ being the voltage peak of the input signal.

If we consider that the necessary swing equals the forward voltage of the base to emitter junction of the transistor, $V_{BE}$, we get the following interval of time $t_D$ before transistor $Q_1$ gets into operation:

$$t_D \approx \sqrt{\frac{\tau V_{BE}}{\omega_A v_i_0}}$$ \hspace{1cm} (9)

For instance, if $\tau = 20\,\text{ns}$ and $v_{PEAK} = 10\,\text{mV}$, it results $t_D = 15\,\text{ns}$ for the case the OA frequency bandwidth is 300 MHz and $V_{BE} \approx 0.6\,\text{V}$. In this condition a large part of the signal information is lost. To overcome this problem we have realized the circuit of Fig. 9. The first feature of the circuit is the use of Schottky diodes instead of standard pn junctions diodes. The smaller threshold voltage of Schottky diodes ($\approx 0.3\,\text{V}$) allows saving dead time. In addition, diode $D_2$ and resistors $R_{D1}$ and $R_{D2}$ have been added to bias diode $D_1$ close to its forward working condition. As soon as the input signal starts, the OA output at node B does not necessitate any jump to put $D_1$ into operation. If resistor $R_B \ll R_{D1}$ the output voltage remains close
to zero at DC. We have the result that

$$V_{\text{OutDC}} \approx \frac{V_T}{1 + \frac{R_D}{R_B}} \ln \left( \frac{-V_{\text{EE}}}{V_{\text{OutDC}} R_D} \right)$$

(10)

$V_T$ being 26 mV at 300 K. By assuming $R_{D1} = 11 \ \text{K} \Omega$, $R_B = 200 \ \Omega$, $R_O = 100 \ \Omega$, and $V_{\text{EE}} = -5 \ \text{V}$, it results that $V_{\text{OutDC}}$ is closed to 1.2 mV and the static current in $D_1$ results about 10 $\mu$A. Since for this biasing condition the threshold voltage for $D_1$ has become close to zero volts the time lag is almost eliminated. Let us consider also the presence of a large rate of incoming signals. In this case there is the possibility that a signal piles up on the tail of the previous one. For this case the BLR may be in the discharging state with $D_1$ cut off and $D_4$ forward biased. Under this condition, the output node of the OA should jump promptly by two forward diodes voltage to cut off $D_4$ and to turn on $D_1$. To reduce the amplitude of the step to only one forward diode the network composed of $D_3$, $R_{D1}$, and $R_{O2}$ is included. With this solution $R_{D1}$ must be small enough to allow the sinking of the discharging current from $D_4$, the choice was 1.6 k$\Omega$.

Results obtained have been very good as can be seen in the scope pictures of Fig. 10. In the figures the input signal is negative and inverted at the scope screen. The response of the BLR to a 20 ns RC-CR impulse is shown for both small and large signals. In both cases the signal is read at the receiving end of a 50 $\Omega$ coaxial cable terminated at both ends. The BLR output signal is superimposed to the input signal. The AC coupling time constant has been chosen about 8 times the shaping time to minimize the noise due to the BLR [13]. As can be seen, the signals at the output of the BLR, the shorter ones, do not show any missing or distorted part. This is evident also from the integral-linearity measurements shown in Fig. 11. The integral error is within 0.4% in the 3 V range. Measurements have been done with a RC-CR signal shaped at
20 ns. The OA used was an OPA655 by Texas Instruments and the supply voltage was ±5 V.

Finally, it has also to be remarked that the BLR described needs only a very small space occupation, thanks to the small number of components used. The circuit of Fig. 9 has been laid-out in a very small board, 19 × 12 mm², see Fig 12.

2. Conclusions

A new Baseline Restorer circuit (BLR) has been realized. The circuit has been optimised for any condition of operation, static and dynamic, and to face both large frequency response and very small frequency response. Signal shaped with filtering time constant as small as 10 or 20 ns are easily supported.

For these circumstances the signal rate can be as large as 10 MHz, with large pile-up percentage. The integral linearity is very good, being less than 0.4% in the 3 V range of a system having ±5 V power supply.

Applications where the speed of response is very slow, like bolometric detectors, exploit the realized BLR, too. For instance, the experiment CUORICINO, consisting of an array of 70 bolometric channels, uses this BLR for the generation of the analog trigger. A simple network has been further added to the BLR to cancel the presence of the re-trigger effects that comes from large signals that have undershoots.

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References

Reference [12]:

Abstract—We present a very precise and stable pulse generator to be used for the calibration of an array of large mass bolometric detectors. The realized instrument is characterized by the presence of multi-outputs and is completely programmable in pulse width and amplitude. Triggering is allowed with a dedicated line. Although featuring \( \frac{1}{1000} \) stability, it was realized exploiting commercial devices, obtaining a very cheap solution.

Index Terms—High stability, low thermal drift, programmable circuits, pulse generation.

I. INTRODUCTION

The first step toward the realization of the 1000 channels experiment CUORE (Cryogenic Underground Observatory for Rare Events) is starting. It consists of 62 large mass TeO\(_2\) bolometric crystals, 790 g each [1]. The intention of the experiment is to study the neutrino-less double beta decay of \(^{130}\)Te contained as an isotope in the TeO\(_2\) [2].

A bolometric crystal converts the energy released by the impinging particle in a temperature increase, that is readout by a thermistor glued on it. The developed signal is very slow, having a few Hz bandwidth, but at the same time the expected signal rate is very low, a few tens of mHz.

Bolometers are very resolving detectors [3], [4]. Our devices show an energy resolution that spread from 6 eVFWHM to 12 eVFWHM per gram of mass at 2.5 MeV of particle energy.

The experiment we are going to start must take data for at least two years. The stability of the energy conversion gain is of great importance. To calibrate, and maintain calibration with time of the whole apparatus is of the heating resistor, for which we defer its description to [5], and to the pulse generator. The instrument we are presenting, although very stable, is obviously not an absolute reference and a periodical use of a source of particle should anyway be needed to re-calibrate the system.

In this paper we describe the solution adopted in the realization of a very stable, multichannel outputs, reference, pulse generator. Results obtained will be shown in detail.

II. CALIBRATION PULSE GENERATOR SPECIFICATIONS AND PRINCIPLE OF OPERATION

The detector array is composed of a tower having 16 floors. On each floor 4 detector crystals are allocated. The heating resistors of every crystal that stay on a floor are all connected in parallel.

It is foreseen to send calibration signals in sequence, one floor at a time. The amplitude of the signal must be selectable to be able to calibrate each detector on its full dynamic range. The acquisition system must decide when and to which floor to send the signals. The amplitude of the signal sent is also read back by the acquisition system. The ratio of the signal read at the output of the detector’s front-end, second stage and acquisition system chain and the signal sent is free or highly immune from any drift of any part of the chain.

The calibration signal is a square pulse having a width much shorter than the detector signal. For the detectors of CUORE the range is between 500 ns and a few ms. The bolometers are sensitive to the energy developed across the heating resistor. The parameter of interest is the quantity \( E_G = V_G t_W (J \Omega) \), where \( V_G \) is the pulse amplitude and \( t_W \) its width. \( E_G \) is an energy referred to 1 \( \Omega \). The heaters glued on each detector have resistance value ranging from about 50 K\( \Omega \) to 100 K\( \Omega \). The calibrating signal should satisfy

\[
V_G = \sqrt{1.6 \times 10^{-10} R_H t_W / \alpha U_C (eV)}
\]  

(1)

where \( R_H \) is the resistance of the heater, \( U_C \) the wanted calibrating energy expressed in eV, and \( (1 - 1/\alpha) \) a parameter that accounts for any amount of the given energy lost because of the thermal conductive path toward the heat sink due to the connecting wires. As an example considering an \( \alpha \) factor of about 5, \( R_H 100 \Omega \) and \( t_W 1 \) ms, \( V_G \) should range from 2.8 mV to 9 mV for energy calibration pulses from 100 KeV to 1 MeV.
The schematic that illustrates the principle of operation of the pulse generator is very simple and it is shown in Fig. 1. The concept is to deliver a voltage of a precise buffered reference to the heater, when needed. The analog switch SW is used to solve this task: by closing it for the required amount of time it allows energizing the heater. The schematic of the solution adopted minimizes as much as possible any drift or error that can be added to the system. The reference voltage is a commercial device that, as a standard characteristic, needs to be buffered for driving any kind of load. In our case the buffer gain is selectable, as explained in the following sections. To avoid any error due to the possible change with temperature in rise time or slew rate of the buffer itself, SW is used in such a way that the buffer output voltage remains constant and must only deliver the needed current when the system is fired. The only question to debate is the possible effect that can be induced by the charge injection of the switch with respect to the buffer capability. This problem and solution will be addressed in the following sections.

III. SCHEMATIC OF THE CALIBRATING PULSE GENERATOR

The pulse generator, Fig. 2, is split into two parts, according to the system requirements. The detector array is inside a refrigerator that is surrounded by a Faraday cage. The circuitry that generates the analog pulses, the analog-mixed boards of Fig. 2, is in a rack located on the top of the refrigerator, inside the Faraday cage. The ‘analog-mixed boards’ have a slow clock that is idle when not addressed. The main precise 10 MHz clock used to determine the pulse durations is always running for maintaining maximum stability. For this reason it is put outside the Faraday cage to minimize EMI interference. The “analog-mixed boards” communicate with both the oscillator card and the computer via two optical links.

In the following subsections we will describe in detail each of the blocks that compose the system of Fig. 2.

Let us start to describe the ‘analog-mixed boards.’ Each of them are laid-out on a four layers Printed Circuit Board that measures \(100 \times 220\) mm\(^2\) (standard Eurocard).

The schematic of any realized ‘analog-mixed board,’ the core of the pulse generator, is shown in Fig. 3. The block ‘V-ref generator’ contains the voltage reference, a heavily low pass noise suppressor filter, and a buffer amplifier. Between this block and the output stage there is the ‘Amplitude selector’ block that allows attenuating the reference level to the wanted amplitude. This block determines the coefficient \(\beta\) of Fig. 1. Every ‘Output stage’ block of Fig. 3 includes a switch SW of Fig. 1 and some additional circuit elements. Each ‘analog-mixed board’ has four ‘Output stages’ to serve four heaters. To feed the whole array four of such boards are therefore needed. A ‘Thermal compensation’ section is included for a fine adjustment of the overall drift.

The ‘Selector’ block allows the acquisition system to read back some selected node voltages of the circuit.

A Complex Programmable Logic Device, CPLD, regulates the functional behavior of the board. It communicates with the computer via a fibers optic synchronous serial bus, buffered by the Digital trans/receiver block. From the computer it receives the commands to determine the pulse amplitude, the pulse width and which output to fire. The triggering of the signal is also generated by the CPLD after the external Clock signal is switched on.

Let us explode now in more detail the main blocks.

A. The V-Ref Generator

The ‘V-ref generator’ is shown in Fig. 4. The Voltage reference is the 5 V generated by the LT1027 (Linear Technology). A heavy low pass filter, \(R_L\) \(-\) \(C_L\), is connected at its output to attenuate the noise. \(R_L\) and \(C_L\) have been chosen to maintain completely negligible any possible effect of the leakage current of \(C_L\).

The Operational Amplifier, OA, \(A_1\) TLE2071, buffers the output voltage.

The Trim input pin of the LT1027 is exploited to add a voltage Proportional to the Absolute Temperature, PTAT, of an amount dependent on the selection of resistors \(R_1\) and \(R_2\), on the basis of the voltage applied to the node \(A_T\). Resistors \(R_3\) and \(R_4\) are fixed at the value of 5.1 k\(\Omega\). The PTAT voltage allows to compensate...
Fig. 3. Complete schematic of the analog-mixed board. The clock generator is remote and communication is via optical fiber link.

the thermal drift of this block, specified to be about $\pm 2 \text{ ppm/}^\circ\text{C}$ (typical), and of the following circuit elements, as will be illustrated in Section III-D.

B. The Amplitude Selector

The ‘Amplitude selector’ block circuit diagram is shown in Fig. 5. It consists of a very precise and low drift R-2R Digital to Analog Converter, DAC, AD7545A from Analog Devices. The DAC input reference voltage is the output node A of Fig. 4. This DAC is not buffered internally, so we added the OA $A_2$ to perform this action. The necessary feedback resistors for the inverting configuration of $A_2$ are provided by the DAC itself. We have indicated the equivalent schematic of the DAC. Resistor $R_f$ is fully matched with any resistor combination $R_A, R_B$, that changes for every setting of the DAC. The resulted specified overall typical thermal drift is $\pm 2 \text{ ppm/}^\circ\text{C}$.

The output of $A_2$ is inverted by $A_3$ to have positive polarity at the output $C$, as required. Resistor $R_t$ and capacitance $C_t$ add a small compensation to the buffering action of $A_3$. The two inputs $A_{1,2}$ allow to set an appropriate PTAT voltage for correcting the drift of the OAs $A_2$ and $A_3$, both part of a dual OP270 by Analog Devices.

C. Output Stage

The ‘Output stage’ circuit is shown in Fig. 6. It consists of a resistive attenuating network that reduces the signal present at the input node $C$, connected to the corresponding output node $C$ of Fig. 5, to the fraction required to produce across the heater resistor the needed calibrating power. Three different attenuation levels are selectable remotely by the analog switches Atten.$i$ to Atten.$3$, ADG452 (Analog Devices). Whatever is the output selected, the output impedance is in any case close to 150 $\Omega$. This attenuator is realized by using very stable and precise resistances and has less than 1 $\text{ppm/}^\circ\text{C}$ drift, see following Section III-D.

In this stage the output pulse is created. In normal condition of operation switch Gnd is closed, switch Signal is open, and one of the switches Atten.$i$ is closed. Therefore the output is at ground potential. This connection to ground is realized only with passive components, avoiding the presence of any possible DC offset. This condition is a very stringent requirement as any DC offset would generate a constant heat injection that should increase the detector temperature. Furthermore this solution allows a great suppression of cross-talk from any other, eventually, fired output.

If a pulse is to be given, the CPLD opens promptly the switch Gnd and closes the switch Signal of Fig. 6, for the amount of time, $t_{\text{on}}$, needed to create the pulse. The output node $C$ of Fig. 5...
is then connected to the OUT node of the ‘Output stage’ via the resistive attenuator, to feed the heater resistor at the appropriate voltage level. As soon as the pulse duration, \( t_{\text{ON}} \), is finished the CPLD opens again the switch Signal and closes the switch Gnd to ground.

The analog switches Gnd and Signal work in anti-phase, minimizing any injection across \( R_{\text{th}} \). Capacitance \( C_f \) is also added to filter any possible residual glitch. The output rise and fall time of the signal pulse are limited to about 900 ns.

An important consideration concerns the switch Signal, since its on-resistance may add a nonnegligible drift. The analog switches used are the ADG452. Four switches are accommodated on a single integrated circuit. The on-resistance of any of these switches is about 6 \( \Omega \) at the supply voltage adopted (0, +10 V), and has a drift of about 3500 ppm/K. The switch Signal has been actually implemented by putting the four switches of one ADG452 in parallel, obtaining the final value of 1.5 \( \Omega \). At first approximation the contribution to the drift coming from Signal is proportional to the ratio of its on-resistance and the output resistance \( R_{\text{th}} \), 20 K\( \Omega \). The maximum effect to the output drift coming from the realized combination is about 0.26 ppm/K.

D. Thermal Compensation

The ‘Thermal compensation’ schematic diagram is in Fig. 7. It consists of an analog thermometer, the LM50B from National Semiconductors, connected to two buffer amplifiers for obtaining two voltages of opposite sign, proportional to temperature.

The two voltages are able to compensate drift of any polarity. The LM50B generates a voltage linearly dependent on temperature having a slope of 10 mV/K. Its output voltage has an offset of about 800 mV at 300 K. We cancel this offset with proper value of resistors \( R_{\text{T1}} \) and \( R_{\text{T2}} \), which scale VREF. This offset adjustment determines the feedback of \( A_4 \) to have a voltage gain slightly larger than one. The final Pos.Tem. and Neg.Tem. slopes are about 12 mV/K.

The Thermal Correcting nodes of the board can refer to one of the two outputs Neg.Tem. and Pos.Tem. via a selected series resistor as follows.

If \( V_{A1h}, V_{DAC1h}, V_{A2th}, \) and \( V_{A3h} \) are the voltage drifts of node A of Fig. 4, the DAC of Fig. 5, and the two OAs \( A_2 \) and \( A_3 \) of Fig. 5, respectively, then at node C of Fig. 5 we expect a total voltage drift of

\[
V_{\text{Cth}} = \frac{R_F}{R_A} (V_{A1h} + V_{DAC1h} - V_{A2th}) - \frac{R_F}{R_B} V_{A2th} - V_{A2th} + 2V_{A3h}.
\]

The value of resistors \( R_A \) and \( R_B \) inside the DAC change for every selected value of the DAC output. This means that \( V_{\text{Cth}} \) is composed of the sum of 4 terms, the last 2 of which are not dependent on the value of the output voltage selected.

To determine the value of the compensation resistor \( R_{\text{T1}} \) of Fig. 4 and resistors \( R_{\text{G1}} \) and \( R_{\text{G2}} \) of Fig. 5 that should be connected to nodes Pos.Tem. or Neg.Tem. of Fig. 7, we adopt the following procedure. The voltage drift \( V_{\text{Cth}} \) is measured in 2 different working conditions for the DAC, putting the analog-mixed board inside an environmental chamber, and varying its temperature. The first measurement is performed when the DAC output is set at its maximum value. The voltage at node B of Fig. 5 is equal to

\[
V_{B_{1\text{max}}} = \frac{R_F}{R_{\text{AFS}}} (V_{A1h} + V_{DAC1h} - V_{A2th}) + \frac{R_F}{R_{\text{BFS}}} V_{A2th} + V_{A2th}.
\]  

where \( R_{\text{AFS}} \) and \( R_{\text{BFS}} \) are the value that \( R_A \) and \( R_B \) of Fig. 5 have for this DAC setting. In the second measurement the DAC output is put at its minimum value, that coincides to the case \( R_A \) and \( R_B \) form an open circuit. In this situation we can make the following discriminations:

\[
V_{B_{2\text{min}}} = V_{A2th} + 2V_{A3h} - V_{B_{2\text{th}}}.
\]

The DAC used is of R-2R type. When it delivers its maximum output, a factor of \( \gamma \approx 1/3 \) for the ratio \( R_F/R_{\text{BFS}} \) can be calculated and \( R_F/R_{\text{AFS}} \approx 1 \). From the \( \gamma \) term, (3) and (4) we have all the necessary parameters to calculate the compensating resistors

\[
V_{B_{1\text{th}}} - V_{B_{2\text{th}}} = \gamma V_{B_{2\text{th}}} \approx \frac{R_F}{R_{\text{AFS}}} (V_{A1h} + V_{DAC1h}) = \pm V_{TH} \frac{R_F}{R_{\text{AFS}}} \frac{R_{G}R_{3}}{R_{G}R_{3} + 2R_3}. \]

\[
V_{\text{TH}} = \frac{12 \text{ mV}}{\text{K}}.
\]

The factor \( \lambda (\approx 21.2 \times 10^{-3}) \) is the ratio between the voltage at node A and node T of Fig. 4, and \( R_3 \) is equal to \( R_4 \). The sign to be used in the above equation determines if \( R_1 \) should be connected to the nodes Pos.Tem. or Neg.Tem. of Fig. 7. In a similar way we have

\[
V_{B_{2\text{th}}} = \pm V_{TH} \frac{R_{c2}}{R_{G2}R_{G1}}.
\]

As can be observed the resistor values determined for the thermal compensation are not dependent on the code selected in the DAC. As a consequence, the compensation is effective above the full range of output voltages. The compensation circuit realized has a large efficiency. In addition, the drift present before compensation is already small. As a consequence, even a hypothetical, very far condition, 10% of compensation error due to device tolerance, aging, and so on, will result anyway.
in a final drift of less than 1 ppm/°C, well within the required specification.

Switch Signal of Fig. 6 has been shown to add a negligible contribution, \( \pm 0.2 \) ppm/°C. The resistors used to implement the attenuator of Fig. 6 are very stable resistors.\(^1\) We measured them in the temperature range 5°C ± 40°C. Results are shown in Fig. 8 and Fig. 9.

As can be seen from the histograms it was possible to select and match the attenuators needed with an accuracy close to 0.5 ppm/°C. Therefore, we decided to not compensate also for the contribution to the overall drift coming from the network of Fig. 6, since already small enough.

All the calibrations have been done with a VT7004 by Vötsch environmental chamber and the Keithley 2700 multichannel input 6 1/2 digits Voltmeter. The temperature range considered for the test were the interval 5°C ± 40°C.

E. CPLD-Firmware

The description of the operation of the firmware of the system is based on the scheme of Fig. 2.

The ‘Clock generator card’ is used to generate the precise time reference for the construction of the analog pulse signals at the analog-mixed board outputs.

This circuit is based on a crystal oscillator module working at 10 MHz. The oscillator has a specified frequency stability of \( \pm 50 \) ppm over its 0–70°C operating temperature range and for supply voltage in the range 5 V ± 0.25 V. A CPLD is present on this card to provide the communication with the other elements of the system.

The input and output communication signals are transmitted using Fiber Optic (FO) lines, that avoid ground loop and/or the conduction of EMI interference inside the Faraday cage. The operation of the circuit is very simple. The CPLD polls the Clock Request FO line and the Trigger Line. When both are found high a clock signal is generated, proportional to the 10 MHz oscillator, and sent at the Clock FO line. The period of the clock output was determined to be 100 \( \mu \)s with 10% duty cycle, 10 \( \mu \)s of pulse width. This clock signal terminates when the analog-mixed board completes the generation of the analog pulse. The analog-mixed board notifies this condition by clearing the Clock Request signal.

The analog-mixed board operation is as follows.

All its necessary settings come from a further CPLD, see also Fig. 3. The firmware of this CPLD has been developed using Very high speed Hardware Description Language, VHDL. In the VHDL description, two main blocks are implemented.

The first block, the bus manager, controls the FO lines synchronous serial bus, SDA and SCL, used to communicate with the acquisition system. It polls these synchronous serial bus signals and, when activated, de-serialize the data line to the 8 bits internal parallel bus of the analog-mixed board, or serialize the 8 bits internal parallel bus to the data line. Since many analog-mixed boards compose the system, each analog-mixed board has its own address and the protocol of communication is addressable from the remote system.

The second block, the board manager block, has a double task. It allows the proper setting of the analog-mixed board on the basis of the pattern received remotely and provides the commands for the generation of the analog output pulses. It needs four bytes to configure the analog-mixed board. The first byte is for the determination of the analog pulse width to be generated. The number stored in this cell gives the analog pulse width in units of 100 \( \mu \)s. The pulse width can then be as long as 25.5 ms. A second byte contains the eight less significant bits of the 12 bits of the DAC. The third byte is divided in two parts, the four LSBs are the most significant bits of the DAC. Bits 5 and 4 select which of the four possible outputs of the board must be fired if bit 6 is 0, otherwise (bit 6 = 1) they address the selector of Fig. 3. The auxiliary analog output can be the reference voltage present at node A of Fig. 4 or the signal present at node C of Fig. 5. Bit 7 asks for the generation of the pulse when set equal to 1, if bit 6 is 0. It is auto-cleared when the pulse is finished. The fourth byte is used to select the output attenuation of each of the four channels present on the board. The byte is divided in four pairs of bits, one for each of the four channels present on the analog-mixed board. As can be seen in Fig. 6 there are only three possible attenuations selectable. The
remaining code of each pair of bits is dedicated to the disconnection of the respective output, when selected.

The generation of a pulse is as follows. The remote system sets the first 3 bytes of the analog-mixed board. The fourth byte needs to be set only once, at the start of the data tacking. If bit 7 of the third byte is 1, the analog-mixed board set the Clock request FO line. When the Trigger line is also set by the remote system the ‘Clock generator card’ outputs the 100 µs clock on the Clock FO line. On the first occurrence of the Clock a counter starts in the analog-mixed board, counting the number of period stored in the first byte configured. At the same time the selected analog output of the analog-mixed board is connected to node C of Fig. 5. After the pulse is finished the Clock request is cleared and the boards goes in the idle state. When a pulse generation is in progress all the write operations are disabled to avoid errors.

For all of these operations the CPLD present on the analog-mixed board uses two clock sources, a 500 KHz clock from an on board R-C oscillator, NE555 based, and the 100 µs clock described above, from the external Clock FO line.

The 500 KHz clock is used for the serial bus communication and for the board setting. It is normally idle and is waken up when either SCL or SDA lines change from their idle state. The 100 µs clock is the precise reference for the definition of the analog pulse width. It is generated and received on the Clock FO line only when the Clock request and Trigger lines are set from the analog-mixed board itself and the remote system, respectively.

In Fig. 10 the schematic diagram of a bi-directional FO single line used for the synchronous serial bus is shown. It is implemented with two FOs. An Infineon SFH551 converts the signal received from light to TTL, open collector. A Schmidt trigger stabilizes the speed of response. A MOS allows sending back the data on the line. A second FO reads back the data converted from TTL level to light by a buffered Infineon SFH756. In case the line is mono-directional the sender FO and the MOS are not present. Resistors $R_T$ are for line termination and $R_P$ is the pull-up resistor. In Fig. 10 the part of the circuit inside the box is the light to TTL trans/receiver of Fig. 2.

The implementation of the above-described synchronous FO serial bus uses four FOs to operate.

IV. MEASUREMENT RESULTS

The accurate characterization of a precise instrument is a very difficult task. The energy given by the pulse generator is proportional to both its width and the square of its amplitude. The pulse error can be expressed in first approximation as

$$\frac{\Delta U_C}{U_C} = 2\frac{\Delta V_G}{V_G} + \frac{\Delta t_W}{t_W} - \frac{\Delta R_H}{R_H}$$

with $U_C$, $V_G$, and $t_W$ defined in (1). We concentrate on the evaluation of the first two terms of the above equation.

The accuracy of the stationary amplitude of the output signal, after thermal compensation, has been obtained under the condition that the switch Signal of Fig. 6 remains always closed during the measurement. During all the tests the ‘Clock generator card’, the ‘Light to/from TTL card’ and the ‘Analog-mixed board’ of Fig. 2 were put inside an environmental chamber the VT7004 by Vötsch. Measurements have been done with a 6 1/2 digit multimeter, Keithley 2700.

Results have been very good. As a typical example we show in Fig. 11 the drift at the output at the Atten. 3 pin of Fig. 6. In the Fig. it is shown, left axis, the output of Atten. 3 after its settled average value of 12 mV has been subtracted. The two horizontal lines superimposed on the curve are were the drift has been extrapolated. On the right axis the corresponding output of the Pos.Tem. of the thermometer of Fig. 7 is shown for reference. The temperature at the output stabilized at 5°C from counts 20 to counts 40, then was changed to 40°C from count 40. Each count correspond to about 100 s of elapsed time. The drift observed in the measurements is about $-0.6 \text{ ppm} / \degree\text{C}$. A similar figure of merit has been obtained for all the other outputs.

The pulse width may change with temperature. We have made measurements with the purpose to estimate its effects. The measurements have been taken for the oscillator and the pulse width at the Atten. 1 output of Fig. 6. Measurements have been made in the following way. The signal was triggered at its start, at half of its amplitude, on the rising edge. Then the time scale of the scope, TDS5052 by Tektronix, was delayed an interval equal to the pulse width. The difference between the start time and the stop time, measured at half amplitude of the signal, were considered equal to the width of the pulse.
Since the pulse generator can give arbitrary pulse width in the range 100 μs to 25 ms, this procedure was repeated at different pulse widths, to study the behavior. The measurements have been taken at 5°C and 40°C. The set-up described allows us to have a precision of the measurements that we estimate about ±0.5 ppm/°C. In Fig. 12 a photograph is shown of the falling edge, at the end of the pulse, for one of the measurements taken at the Atten. 1 output at 40°C.

The final drift of the oscillator resulted limited by our sensitivity, ≤ 0.5 ppm/°C.

The signal width at the output Atten. 1 showed a drift of about 1 ppm/°C in the more stringent condition of 100 μs of pulse width, 0.1 ms/t\text{FW}(ns) ppm/°C. It has to be considered that the change of the width of the pulse is independent from the width itself. The two results prove that the oscillator does not contribute to the drift of the pulse width. We have anyway verified the thermal drift of the oscillator adopted. We measured its frequency with a HP53132A (225 Mhz Universal Counter) at 5, 10, 20, 30 and 40°C. The maximum value measured was 0.12 ppm/°C.

So far we have described results obtained when the amplitude of output voltage is measured at DC and the pulse width is measured at a determined threshold. One other source of possible error may arise if the rise or fall time of the signals change, for instance due to the settling time of the OA A3 of Fig. 5 when forced to change the driving current promptly. This phenomenon is correlated with the pulse width drift. As a worst condition we have considered the two effects anyway as independent. We have measured the rise and fall time changes with temperature and verified that the fall time remained practically constant within the temperature range between 5°C and 40°C. Its variation was only a few nanoseconds above 880 ns. This features was expected since the signal fall time is governed only by the discharging of the filtering capacitance C_f of Fig. 6 with the resistors connected to it. The rise time changed about 25 ns in the temperature range considered. This is mainly due to the settling time of the OA A3 of Fig. 5. It is very easy to quantify the error that comes from the rise time change. The rise and fall times of the signal pulses of the circuit implemented are free from any overshoot or undershoot and governed by a simple exponential time constant for both edges. A pulse of unitary amplitude can therefore be modeled as

\[ V(t) = \begin{cases} 1 - \exp \left( -\frac{t}{\tau_r} \right) & 1(t) \\ 1 - \exp \left( -\frac{t - t\text{FW}}{\tau_f} \right) & 1(t - t\text{FW}) \end{cases} \]

(8)

where \( \tau_r \) and \( \tau_f \) are the time constants for the rise and fall time, respectively. The energy given to the heater is proportional to the square of (8). If we suppose that only the rise time drifts we easily obtain (F is for final, I for initial)

\[ \Delta E = \int_0^{+\infty} [V(t)^2]_F - [V(t)^2]_I dt \approx \frac{3}{2}[\tau_f - \tau_r] \]

(9)

where in the last equation it has been considered that the rise time \( t_r \) equals 2.2 times the time constant \( \tau_r \). The rise time drift has been measured over a range of 35°C. From (9) we therefore get about 0.485 ns/t\text{FW}(ns) ppm/°C of drift in the energy as only the rise time fluctuates with temperature. The drift considered is independent of the pulse width, therefore it increases its effect at the smaller pulse width.
Fig. 13. Noise jitter of a 100 µs pulse width at the Atten.1 output. The jitter of the pulse was measured triggering the scope on the signal raising edge and then sampling the falling edge shown after a delay of 99.9 µs. The vertical scale is 10 mV/div and the horizontal one is 200 ns/div. The measured pulse duration has a σ of 3.33 ns.

We have measured also the noise due to the jitter of the width of the output pulses. In Fig. 13 there is a photograph where the histogram of the jitter of the falling edge is measured, after the signal has been triggered on the rising edge. Due to the limited memory available on the scope and for the required high sampling rate, to get enough time resolution we delayed the sampling window shown by 99.9 µs. The trigger level was set at about 20% and the jitter was evaluated at about 80% of signal amplitude.

Another issue is the long term stability. The circuits components we have used have specified, on the average, a few tens of ppm/month in their first period of life. To try to limit this performance to a few ppm/month we aged the realized circuits by warming them at about 50°C for days. This together to the periodical (monthly) use of a particle source, should allow to maintain the overall system stability within the limits showed above.

V. CONCLUSION

A very precise and stable pulse generator for an array of bolo-metric detectors has been realized. It is able to generate square pulses having maximum programmable amplitude that, after resistive divider, is 40 mV, with 12 bits of resolution. The width of the pulse can be set between 100 µs and 25 ms. All the features of the realized instrument can be programmed remotely with a fiber optic synchronous serial bus.

The drift of the amplitude of the pulse was less than 1 ppm/°C. The drift of the pulse width, ∆t, was about 1 ms/∆t (°C) ppm/°C + 0.1 ppm/°C. Concerning variation of the rise/fall time duration, it was verified a drift of 0.5 ms/∆t (ms) ppm/°C. The drifts have been measured in the temperature range 5°C to 40°C.

The noise due to the jitter was about 3.5 ppm RMS at 1 ms of pulse width.

By supposing a possible change of the room temperature of about ±5°C, we expect, as a worst condition, 35 ppm (or 87.5 eV at 2.5 MeV) of absolute precision of the calibrating signal at 1 ms pulse width. This figure is much better than the expected detector resolution, which is about 850 ppm RMS (5 KeV FWHM at 2.5 MeV particle energy as a best condition).

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REFERENCES

Reference [13]:

Low-noise, low drift, high precision linear bipolar (±10 V) voltage supply/reference for cryogenic front-end apparatus

Gianluigi Pessina
INFN Istituto Nazionale di Fisica Nucleare, Dipartimento di Fisica dell’Università di Milano,
Via Celoria 16, 20133 Milano, Italy

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A very simple linear bipolar (±10 V) voltage supply/reference (VS/R) featuring very low noise has been implemented. The noise is about 1 μVpp in a 0.1–10 Hz bandwidth, becoming, for the −10 V supply only, 1.3 μVpp at 1.5 A. The VS/R is based on commercial devices and has been designed to face the stringent requirement of very low drift systems. It features very good line regulation, less than 10 mV over 10 V at 1.5 A supply current, and very low drift, between 3 and 8 ppm/°C; it also shows large power supply rejection ratio (PSRR), >120 dB. The VS/R presented includes also safety circuits, to protect itself and the electronic equipment to be supplied in an actual experimental condition. It is protected against inversion of polarity and against under and over voltage at its inputs, and has a foldback current limiting circuit which shuts down the whole system if the current absorption lasts for some time. These protecting circuits acts on both outputs (±10 V), to maintain always the symmetry. From an analysis made on the data extracted from the measured noise spectra, it was possible to measure the dynamic output impedance, found mainly inductive, with a value of the order of 1 mH. The dc PSRR has been improved by about 20 dB with respect to the performances of the devices used, thanks to a very simple circuit solution. © 1999 American Institute of Physics.

I. INTRODUCTION

The front-end electronics for cryogenic bolometric detectors needs to be very accurate not only for what concerns the noise performances, but also for precision and low drift. The preamplifiers which readout the detector signals are realized using hybrid solutions, where discrete and monolithic devices share a common substrate. Low drift systems are obtained if the direct current (dc) voltages and currents of the working points are very precise and show low noise, especially at low frequencies. These tasks can certainly be obtained, saving space occupation, if the voltage supplies used for the preamplifiers and the subsequent stages can be used at the same time also as very precise reference voltages with low noise and low drift. This way a detector having a large number of channels can be equipped with a few such voltage supplies, located near a suitable number of readout channels.

In this article, a linear voltage supply designed and realized for this purpose is described. In the following sections, the basic diagram of the voltage supply will be introduced. In Sec. III, the part of the circuit devoted to the protection against wrong input connections and under/over voltage will be described. Finally, in Secs. IV and V, the schematic circuit and the current limiting protection circuit and the experimental results will be shown.

II. THE SUPPLY VOLTAGE SYSTEM

The front-end electronics for bolometric detectors has to be very stable against ambient temperature variation. Very often the very front-end preamplifier is realized with an hybrid circuit consisting of discrete and monolithic devices, which may need an accurate reference current or voltage, common to the whole network, to get an overall stable and precise working point. In these cases, it is a difficult task to realize very precise voltage references, as can be done with a monolithic circuit, but it is possible to use monolithic commercial band-gap voltage references, or zener based references, which exhibit very low drift. Unfortunately, these circuits show also large noise, and this can be very critical because noise can be added to the circuit, unless it is filtered using very large capacitance values.

For this reason, we decided to design a voltage supply that is able to be at the same time also a very precise and low-noise voltage reference. Since we intend to use it with a detector with a large number of channels, the design was aimed at obtaining a very robust circuit, capable of driving a large current and also equipped with circuits that protect it against undesired situations frequently present in an experimental environment.

In Fig. 1, the schematic diagram of the system is shown. The unregulated dc input voltages, $V_{IN1}$ and $V_{IN2}$, are checked for their correct connection to the system. After being filtered, a “decision” network assures the rest of the circuit against possible under or over voltage failures. The resulting pair of bipolar sources, $V_{PAS+}$ and $V_{PAS-}$, are the ones that will be regulated to generate the final ±10 V linear voltage supply/reference, VS/R. To maintain symmetry under all situations a protecting circuit, which acts on both output voltages at the same time, is also included.

III. INPUT SAFE PROTECTION CIRCUITS

Experience shows that it is not so difficult to confuse the connections of the voltages applied to the circuit, in an ex-
perimental condition. A protection against any possible error has been implemented. The supply voltages can be connected to the circuit with either polarity, the circuit itself is able to select the correct output combination. For any other wrong input combination, nothing is transmitted. The behavior of the network is similar to that of the four diodes bridge rectifier, but with a much smaller voltage drop across it. The implementation has been realized in a simple form, using metal–oxide–semiconductor (MOS) transistors as switches. In Fig. 2, the schematic diagram is shown. The MOS transistors used in this network have been operated as shown in the inset of Fig. 2, connected with the source and the drain interchanged, to avoid the effects of the substrate diode Di. With this connection when the MOS is reverse biased, Di is reverse biased too, while when the MOS is forward biased, the low voltage drop between the source-(S’) and the drain-(D’), is very small, and Di has anyway no effect. As a consequence, each MOS behaves as a true switch that autoset itself in a manner explained below. Consider the input voltages with the polarity A of Fig. 2, with V11 positive and V12 negative. The MOS transistors with the label A are in this case all ON. As such, the P-MOS pass transistor Q15 (in ON state), sets the output V+ positive. The N-MOS Q20 forces to be zero the voltage drop between the drain D’ and the gate G’ of the P-MOS pass transistor Q14, putting it in the OFF condition. The same consideration applies to the N-MOS pass transistor Q24, that copy V12 to the negative output V−, while Q23 is put OFF by Q22. If now the input polarity is B, with V11 negative and V12 positive, the transistors in the ON state become all those with the label B. Q14 is the P-MOS that put V+ positive, while now Q15 is set OFF by Q19. The output V− is forced negative by Q23, while Q24 is put OFF by Q21.

The pass transistors used have been selected for their low value of the ON resistance, about 25 mΩ. When the load current is ±1.8 A, the maximum handled by the circuit, the voltage drop across this decision network is only about 0.1 V, to be compared to a value of at least 1 V, which is obtained when using a classical four Schottky diodes bridge.

Another frequent situation happens when the inputs are forced to an over or under voltage condition. This situation occurs especially when the line is filtered with inductances and capacitances. To protect against failures, a pair of window comparators has been used in this design.

Some commercial monolithic “detectors” circuits are able to do this job. We have chosen the ICL7665 (by Harris) that has two inputs, with hysteresis, and two open collector outputs. The inputs, amplified with opposite sign, are both compared with a trip voltage of 1.3 V. To realize the voltage window we need, the circuit of Fig. 3 has been implemented. Two ICL7665 have been employed, U5 and U7, to sense the value of V+ and V−, respectively. The voltage window and hysteresis have been realized with the resistances connected to pins 2 and 3, and to 5 and 6 of both U5 and U7.

The two open collector outputs of each detector (pins 1 and 7) are connected together. In this way each ICL7665 behaves as an analog AND discriminator: only if the input voltage is within the window, the output will be in its high state. For the present solution, the two window voltages were set to: (11.5 V, 13 V) and (−13 V, −11.5 V), with an hysteresis of about 1 V. This choice is a compromise between a minimal and maximal drop across the output power transistor.

If V+ lies in its window, U5 puts in the ON state the N-MOS switch Q20. If V− lies in its window, U7 puts in the ON state the P-MOS switch Q19. Using the N-MOS Q23. Switch transistors Q19 and Q20 are connected in series: only when both are ON the pass MOS transistors Q16 and Q25 are put in their ON state (note that Q25 is driven by the inverter Q21). Therefore, the under/over voltage protection circuit operates in such a way that if and only if both inputs V+ and V− are within their own windows, both the outputs Vpa±.
and \( V_{\text{PAS}^-} \) are connected to the rest of the circuit.

In Fig. 3, an input called SHUT is also present. It is driven high when an overload current lasts for some time (see Sec. IV C). When SHUT is high, the N-MOS \( Q_{\text{TRIP}} \) puts low the input of the Analog AND U5, simulating an under voltage state, that, in turn, shuts down the voltages \( V_{\text{PAS}^+} \) and \( V_{\text{PAS}^-} \).

IV. THE BIPOLAR ±10 V VOLTAGE SUPPLY/REFERENCE

A. +10 V voltage supply/reference

Generation of currents and voltages for proper system operation with low drift and low noise is a very critical step in a circuit realization that is based on discrete and monolithic devices. Also very critical is to obtain very large power supply rejection ratio (PSRR). In a system with a large number of channels, the voltage supplies must feed circuits distributed over a large area. Consequently, possible crosstalks can be present if the impedance of the connecting cables is not sufficiently low. In this situation, a better solution is to use several voltage supplies, each one dedicated to a few number of channels. Their realization must occupy the smallest volume, as space is always limited. Our choice was therefore to make a voltage supply capable at the same time to be also a voltage reference having low drift and low noise, as required with bolometer applications.

The adopted approach for the circuit design is based on the use of a very precise and stable monolithic voltage reference, filtered to lower the noise, and then buffered to drive a large current. The schematic diagram of the circuit is shown in Fig. 4. The monolithic circuit U1 is the BB REF102, a very precise +10 V voltage reference with a very low drift, \(-2.5 \text{ ppm/°C} \) over \(-25 \) to \(85 \) °C temperature range. Although it is one of the lowest noise voltage references commercially available, \(5 \mu\text{Vpp} \) in a 0.1–10 Hz bandwidth, our aim was to improve the overall noise performance further. Its output was therefore heavily low pass filtered by means of \( R_2 \) and \( C_3 \). To obtain a low dropout, the buffering of the voltage present on \( C_3 \) was realized with one of the dual operational amplifier (OpAm) OP284, which has low noise and rail-to-rail input/output capability. The output driver is the power P-MOS \( Q_{P01} \). The chosen configuration for the OpAm-\( Q_{P01} \) buffer exploits the negative excursion of the OpAm output, when \( Q_{P01} \) will increase its gate to source voltage to drive large currents.

If needed, the output voltage can be selected to be less than the +10 V nominal value, by proper setting the resistor \( R_{54} \), or larger, by setting \( R_{65} \) and \( R_{66} \). The nominal output value of +10 V is obtained when \( R_{54}=R_{65}= \) open and \( R_{66} =0 \Omega \).

A foldback current limit is included in the VS/R. If the current absorption of the load does not exceed \(1.8 \) A transistor \( Q_1 \) is off, since the voltage drop on \( R_{51} \) is not enough to forward bias its base-emitter junction, \( V_{BE} \). In this condition, \( Q_{13} \) is ON and \( Q_{14} \) OFF: the network is in its normal mode of operation. If there is a current overload, \( Q_1 \) starts to conduct, limiting the current absorption by putting \( Q_{12} \) in its linear mode of operation, and putting \( Q_{14} \) in its ON state. The OpAm-\( Q_{P01} \) buffer feedback loop stops to operate and the output of U2A saturates towards the negative voltage supply. A foldback effect is also included, realized by using only resistor \( R_{28} \), in series with the switch \( Q_{14} \), and resistor \( R_{53} \). When there is an overload the current limit circuit lowers the output voltage from its nominal value. The consequent flow of current into \( R_{28} \) establishes an increase of the voltage drop on \( R_{53} \). The sum of the voltage drop, V.D., on \( R_{53} \) and \( R_{51} \) determines \( V_{BE3} \). Since the latter is rather constant, the increase of the V.D. of \( R_{53} \) forces the V.D. of \( R_{51} \) to become smaller, decreasing the limit current. If, during the overload, current absorption increases, the output voltage lowers, and the foldback limits the current to smaller and smaller values. As an extreme situation, if a short circuit at the output is present the current is limited only to about 80 mA, maintaining low the power dissipation on \( Q_{12} \). The limiting circuit breaks the buffer feedback loop OpAm-\( Q_{P01} \), and is realized with a loop configuration consisting of only two transistors, \( Q_3 \) and \( Q_{12} \), with a good margin of stability. The presence of the switch \( Q_{14} \) allows to minimize the latchup to the lower limiting current, otherwise fired by the foldback circuit at the startup, or after there has been, for the first time, an overload.

A further protecting circuit is present. When the overload is established, the TRIP\(_{3+} \) node goes high, starting a tripping timer (see Sec. IV C) which shuts down all the system if the overload lasts for more than about 2 s.

Resistors \( R_{19} \) and \( R_4 \) have the purpose to limit the current into the OpAm inputs when it is forced to saturate towards the negative voltage supply, under current overload conditions. Resistors \( R_{19} \), \( R_{19} \), and \( R_3 \) are symmetrically connected at the two OpAm inputs to compensate the drift of the OpAm input bias current. This pair of resistors serves also, together with \( R_{PS} \), for the optimization of the dc power supply rejection ratio of the system, as will be explained in Sec. V.

B. −10 V voltage supply/reference

The circuit of the negative, −10 V, voltage supply is very similar to that of the positive voltage supply. In Fig. 5, the schematic diagram is shown. The input to the network is the regulated +10 V. This voltage is amplified by −1 with the instrumentation amplifier U3, a BB INA105. The
INA105 is especially designed to have unity gain with very low drift and offset. Since the U3 output is not able to reach the negative supply, resistors $R_{11}$ and $R_{12}$ have been added to offset the output of U3 to a few volts above the regulated negative voltage supply. The voltage present at the U3 output, $-10\, \text{V}$, is again heavily low pass filtered with $R_5$ and $C_9$, to eliminate any residual noise present at the output of the INA105. A structure complementary to the one shown in the previous subsection has then been implemented. The second OpAm of the dual chip OP284, U2B, and the driver N-MOS $Q_{10}$ form the buffer stage. The current limiting network is composed of transistors $Q_8$, $Q_9$, and $Q_{11}$ ($Q_8$ and $Q_9$ OFF, $Q_{11}$ ON in normal mode of operation) and resistors $R_{22}$, $R_{21}$, $R_{29}$, $R_{55}$, complementary to those employed for the $+10\, \text{V}$ voltage supply. Even in this case when any overload in current absorption occurs, the TRIP$_{S}$ changes state, starting the timing circuit described in the next subsection.

C. Timing limiting circuit for overload current absorption

A current overload is considered a fault situation accepted only for a transient. As such, if it lasts too long, all supplies are shut down until the normal condition is reached again. This specification has been implemented with the circuit of Fig. 6. The timer U6, a TL7702A, is fired when one or both of the two signals TRIP$_{S}$ and TRIP$_{P}$ change state. In particular, since TRIP$_{S}$ changes from zero to the negative voltage, switches $Q_{17}$ and $Q_{22}$ and resistors $R_{33}$, $R_{39}$ and $R_{40}$ are introduced to translate it into the right positive logic value. The TL7702A is generally used as a startup circuit: when the input increases above its internal reference voltage, it starts to charge capacitor $C_{16}$ until its voltage drop exceeds the same reference voltage, a condition which fires the output to change state. If the input returns to the lower state within the charging interval, the output does not change state. It is then evident how U6 is used in the present application. A current overload will start U6 to charge $C_{16}$. If the overload lasts for more than the charging interval, about 2 s, the output of U6 changes to the high state. When this situation happens, the monostable ICM7555 U8, (a CMOS version of the NE555) puts the SHUT node to the high state for about 2 s. The high state of SHUT shuts down both the +10 and $-10\, \text{V}$ regulated voltages, by closing the switch $Q_{\text{TRIP}}$ of Fig. 3.

The shut down will persist until the overload condition is present, forcing to a negligible value the power dissipated by the output MOS transistors.

V. EXPERIMENTAL RESULTS

As shown above, the presented $\pm 10\, \text{V}$ VS/R has been designed to fulfill several specifications. Firstly, consider the one concerning the noise performance. Noise has been measured at different levels of load current absorption, for both the $+10$ and $-10\, \text{V}$. It was found that noise is quite independent from the current absorption from the load, increasing slightly at the largest currents. At low frequency, the noise spectrum was found to follow a $1/f$ law. For the $+10\, \text{V}$ supply, it resulted to be about 70 nV/$\sqrt{\text{Hz}}$ at 1 Hz. In the frequency bands 0.1–10 Hz (usually used as a parameter of comparison in the data sheets), the peak-to-peak noise is less than 1 $\mu$Vpp, up to 1.5 A load current. The same behavior has been measured also for the $-10\, \text{V}$ supply, except for the current of 1.5 A, where it increases to about 1.3 $\mu$Vpp, with the noise at 1 Hz of 95 nV/$\sqrt{\text{Hz}}$. This behavior can be interpreted by considering the different sources of the parallel noise of the OpAms, U2A and U2B, with their common mode input voltage. The common mode input capability of the OP284 is obtained by using two long tail pairs at the input, one $nnp$ and the other $pnp$. At the positive larger common mode input only the $pn$ pair is operating, while for the negative common mode only the $pnp$ pair is active. The two pairs absorb the same amount of current, when active. For the largest currents the circuit board heats up by about 20–30 °C with respect to room temperature, for the presence of the sensing resistances $R_{51}$ and $R_{52}$ of Figs. 4 and 5. It seems that the low frequency parallel noise of the $pnp$ pair increases with temperature more than that of the $pn$ pair.

Noise spectra for the worst case of 1.5 A load current are shown in Fig. 7, for both the $+10$ and $-10\, \text{V}$ supplies. A slightly larger noise at low frequencies for the negative volt-
The use of a very low drift monolithic reference voltage, along with the strict symmetry adopted in the construction of the buffer voltage, allowed a very low drift system to be obtained, as required by the application. The temperature supply can be noted. It must be remarked that the figure of noise measured is very low compared with that of the commercial monolithic voltages reference, about 5 $\mu$Vpp for frequencies in 0.1–10 Hz range.

As can be observed in Fig. 7, the shape of the noise spectrum is not flat at high frequencies, two plateaus being present, one of which for frequencies larger than about 1 kHz. This behavior is attributed to the output impedance of the VS/R. At dc the output impedance is a few m$\Omega$, but at larger frequencies it shows an inductive component. As can be seen in Fig. 4 at the output of the network a capacitance of 4700 $\mu$F, having in series a resistance of 5.1 $\Omega$, is connected. At large frequencies, a partition between the output impedance of the VS/R and this network is present, that reduces the amplitude of the noise. The residual measured noise is that of the reading preamplifier. In Fig. 8 the circuit model for the described behavior is illustrated. The output impedance of the VS/R is represented by the inductance $L$.

The generator $\varepsilon_{\text{amp}}^2$ represents the series input noise of the amplifier, while the noise of the VS/R is the voltage generator $\varepsilon_{\text{sup}}^2$. At the preamplifier input we expect the noise given by the following transfer function ($s = j\omega$):

$$V_{\text{OUT}}^2 = \left| \frac{1 + sR_C C_G}{s^2 C_L + sC_C R + 1} \right|^2 \varepsilon_{\text{sup}}^2 + \varepsilon_{\text{amp}}^2.$$  (1)

The noise generators were considered to show the following frequency behavior:

$$\varepsilon_{\text{sup}}^2 = \frac{A_f}{\sigma^2} + \varepsilon_{\text{wasp}}^2; \quad \varepsilon_{\text{amp}}^2 = \frac{A_{\text{fam}}}{\sigma^2} + \varepsilon_{\text{wamp}}^2 = \varepsilon_{\text{wamp}}^2,$$

$$A_{\text{fam}} \ll A_f.$$  (2)

The $\chi^2$ method has been used to fit the curves of the measured noise with the model of Eqs. (1) and (2), with free parameters $A_f$, $\alpha$, $\varepsilon_{\text{wasp}}^2$, $\varepsilon_{\text{wamp}}^2$ and $L$. In Fig. 7, the fits for the two noise spectra are superimposed on the curves. The found inductances are 1.9, 1, and 0.8 mH, respectively. A similar result has also been found for the negative voltage supply, with slightly smaller values for the inductance. The results obtained are consistent, once it is considered that the open loop gain of the buffer voltage increases at large currents, due to the transconductance increase of the power output MOS transistor, $Q_{P0}$, and that the output impedance of the VS/R is inversely proportional to the open loop gain of the OpAmp-$Q_{P0}$ buffer.

A last important requirement is to have a large dc PSRR, of at least 100 dB. From Figs. 4 and 5, it is evident that the dc PSRR of the system is limited to the smaller value between the monolithic voltage reference BB REF102, about $\approx 150$ dB, the OpAm OP284, $\approx 90$ dB and the INA105, $\approx 110$ dB. We succeeded to improve the dc PSRR by at least 20 dB with a very simple circuit solution that will be illustrated with a practical example. Suppose that in the circuit of Fig. 4 an increase of the voltage $V_{\text{PAS+}}$ gives origin to a decrease of the output voltage of the positive VS/R with an absolute gain of $-86$ dB, or $-31.6 \mu$V/V. We can compensate this by simply adding a resistor, $R_{P+}$, connected between $V_{\text{PAS+}}$ and the non inverting input terminal of the OpAm-$Q_{P0}$ buffer. The value of the resistor being such that the inverse of its ratio with the corresponding resistor, 5.6 k$\Omega$, connected to the OpAm input equals 31.6 $\mu$V/V. In the example considered, the value of such a resistor would be 177 M$\Omega$. The increase of the dc PSRR is related to the precision of the added resistor. For a minimum 10% accuracy, we expect about 20 dB of improvement.

This technique was applied to the circuit boards realized. The measurement of the residual dc PSRR after correction has required an accurate procedure, since a sensitivity of the order of less than 1 $\mu$V over 10 V was needed. The output voltage of the VS/R under test was attenuated a factor of 2 and sent to one input of a differential amplifier having a
voltage gain of 130. At the other input of the amplifier a voltage reference given by a similar VS/R was connected, to null the offset. The dc output of the amplifier was readout with a HP3572 digital multimeter and stored. The changes in the supply voltage of the VS/R under test and the ambient temperature were also acquired, the latter with a platinum Pt100 resistor. Very good accuracy in the measurement were achieved by taking into account the correlation between the ambient temperature and amplifier output voltage: it has to be remarked than 10 ppm/°C means 100 μV/°C of absolute drift for the VS/R. The obtained result is shown in Fig. 11. The square wave is the supply voltage excitation, the curve with the dots is the measured VS/R response, the continuous curve is the simulation of the VS/R response which accounts also of the ambient temperature variation.

The square wave is the supply voltage excitation, the curve with the dots is the measured voltage response of the VS/R. As can be observed the result is very good, since apparently the VS/R output voltage does not depend on its supply voltage. The continuous curve of Fig. 11 is the fitting of the VS/R. The fitting was calculated with the $\chi^2$ method, assuming a linear dependence of the amplifier output voltage with the measured temperature (changed about half °C over the measurement time), and assuming also a square response superimposed on the VS/R due to the excitation. The interpolation of Fig. 11 has found a peak-to-peak square wave of 0.54 μVpp superimposed on the drift, in response to the 1.2 Vpp input. This corresponds to about 126 dB. The initial dc PSRR for this circuit board was slightly less than 86 dB, and a 100 MΩ resistor was used for compensation.

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Reference [14]:

The Temperature Stabilization System of CUORICINO, an Array of Macro Bolometers

C. Arnaboldi, C. Bucci, S. Capelli, P. Gorla, E. Guarndincerri, A. Nucciotti, G. Pessina, S. Pirro, M. Sisti

Abstract- We present our circuit solution for the implementation of a very simple temperature stabilization system of an array of 62 large mass bolometric detectors, CUORICINO. The implemented instrument exploits one of the front-end channels to close the feedback loop between a thermistor and a heater, both of them located on the detector holder in the refrigeration system. A very compact layout was developed that avoids any possible presence of EMI interferences, otherwise introduced if a commercial instrument were adopted. The stabilized temperature is obtained exploiting the offset correcting circuit of the remotely programmable front-end channel, to auto-generate the reference operating point for the feedback loop. Thank to the adopted configuration the instability of the cryogenic apparatus, which induced a drift corresponding to about 50 keV/day, was reduced to less than about 0.5 keV/day. To model the system behaviour we have reformulated the bolometer theory of operation using the concept of a feed-backed network. The obtained results will be shown.

I. INTRODUCTION

Experiments in high energy physics that must run for long time need always a stabilization system that assures the constancy of the energy conversion gain. The simplest way to maintain a constant gain with high accuracy is to locate a known source of particles close to the detector, allowing a continuous calibration. Unfortunately, often it is not possible to easily tag every signal induced by the calibrating source. This effect may degrade the accuracy in the study of the process under investigation, by adding spurious events to the final energy spectrum.

An experiment performed with an array of bolometers is not an exception to this problem. CUORICINO [1] is an array composed of 62 TeO$_2$ bolometric crystals, featuring 42 kg of total mass. Its aim is to study the Double beta decay, D$\beta\beta$, of $^{130}$Te. Every detector of the array is composed of a TeO$_2$ crystal with volume either $5\times5\times5$ cm$^3$ (790 g) or $3\times3\times6$ cm$^3$ (340 g), depending on the location within the array. On every crystal a Ge NTD [2] thermistor is glued, that converts the thermal increase following the absorption of an impinging particle in an electrical signal. An adequate signal to noise ratio requires very small operating temperatures, closed to 10 mK.

The D$\beta\beta$ is a very rare process. Its study requires very long measurement time and a very low level of radioactive background. Therefore a very accurate stabilization system that does not add background is a stringent requirement. The procedure presently adopted to stabilize CUORICINO is as follows. On a periodic scale, usually once per month, a source of energetic particles is put close to the detector to perform an absolute calibration of the energy scale. Between these periodic calibrations, the monitoring of the baseline of every bolometer allows to account for the temperature of the detector itself and its sensitivity. This condition is met if the front-end does not add drift, as it is the case for CUORICINO [3]. In addition to the baseline monitoring we inject a voltage which develops a power pulse across a special heater [4] glued on every crystal in a proper location, far from the thermistor. The heating pulse simulates the signal generated by an incoming particle. A very stable multi output pulse generator is used to perform this task [5]. The periodic illumination of the detector array with a particle source together with the baseline monitoring and the pulse calibration has given to CUORICINO a very good temperature stabilization [6].

To further improve the stability we have verified that the detector array needs a very high precision temperature stabilization. For this reason a PID (Proportional, Integrative, Derivative) instrument should be used to stabilize the detector holder temperature, inside the refrigerator system. A standard, commercial, solution may be adopted. Some drawbacks of such an arrangement are anyway to be considered. We need to stabilize the temperature around 10 mK using a thermometer with the same level of sensitivity as the Ge NTD thermistors we use, having hundreds of M$\Omega$ resistance value. The standard procedure to stabilize temperature consists in balancing an AC resistance bridge cascaded with a PID controller that closes the loop on a heater. These equipments are in general range limited to few M$\Omega$, due to the presence of shunting stray capacitances. In addition, the usual frequency range of this AC bias (tens of Hz) is in conflict with the bandwidth of our detector signals.

To overcome the mentioned problems we have designed and built a very simple circuit able to stabilize the temperature by simply exploiting one channel of the front-end itself to close...
the loop between the thermometer and the heating resistors. The very important result obtained is that EMI interferences are not injected. In addition the thermometer is operated in the same way as any detector of the array, biased at DC. The operating point is chosen by simply trimming the offset of the channel that, in this circumstance, becomes the reference voltage of the error correcting loop. The setting point is easily obtained thanks to the remote programmability of any channel of the set-up [7].

In the next sections a description of the theory of operation of the stabilization system of the cryogenic array, the complete circuit solution and the experimental results will be shown in detail.

II. THEORY OF OPERATION OF THE STABILIZATION SYSTEM

A. Principle of operation of a bolometer

A bolometer is composed of an absorbing crystal to which a thermistor resistor is attached. At very low temperatures the heat capacity of the absorbing crystal becomes vanishing, according to the Debye law. The thermistor is constructed in order to have high sensitivity. We use Ge NTD thermistors in our experiments, that are well modelled by the function [8], [9]:

$$R(T) = R_o \exp \left( \frac{T_o}{T} \right). \quad (1)$$

Our devices have $R_o$ of the order of a few $\Omega$ and $T_o$ of about 3 K. Using these two values in (1), the thermistor operating points are found around 100 $\mu$K, for temperatures between 5 mK and 10 mK. A very simplified thermal model of a bolometric detector is shown in Fig. 1.

![Simplified thermal model of a bolometer.](image)

Fig. 1: Simplified thermal model of a bolometer.

In Fig. 2 a simulation, performed with Simulink®, of the characteristics of a bolometer read by a Ge NTD thermistor is shown for different base temperatures, from 5 mK to 10 mK. The shape of the I-V curves depends on the value of the thermal conductance towards the heat sink. In Fig. 2 the thermal conductance was supposed mainly due to the gold wires bonded on the thermistor and to the bonds themselves. Their resulting temperature dependence follows the law:

$$K(T) = \frac{\Delta P}{\Delta T} = K_o T^\beta. \quad (2)$$

where $\beta$ equals 2.4 [10] and $P(T)$ is the dissipated power. The background power can be neglected very seldom in these applications. In the simulation shown it was assumed equal to 400 pW.

The larger the thermal conductance, the more the I-V characteristics are expected linear above a larger voltage range. This is visible in Fig. 3 where the simulation includes now the parameter $K_o$ of equation (2) in the I-V curves. Both the behaviours of Fig. 2 and Fig. 3 are a consequence of the so called electro-thermal feedback [11], [12], [13].

![I-V characteristics at different temperatures of a Ge NTD thermistor having $T_o=3.3$ K, $R_o=1.15 \Omega$, a thermal conductance towards the heat sink of $40T^{2.4} \mu$K/W and a background power of 400 pW.](image)

Fig. 2: I-V characteristics at different temperatures of a Ge NTD thermistor having $T_o=3.3$ K, $R_o=1.15 \Omega$, a thermal conductance towards the heat sink of $40T^{2.4} \mu$K/W and a background power of 400 pW.

When a bias is applied, an electrical power flows in the thermal conductance, which rises the bolometer temperature. The temperature increase changes the thermistor characteristics that, in turn, modify the dissipated power itself, closing the feedback loop.

On every I-V curve of Fig. 2 or Fig. 3 the current and the voltage are temperature dependent and correlated to the thermal conductance $K(T)$. The electro-thermal feedback imposes a balance between the temperature and the dissipated power. At any point on any I-V curve of Fig. 2 the thermistor voltage, $V_T(T)$, the thermistor current $I_T(T)$, the dissipated power $P_T(T)$ and the temperature $T$ must be related. Exploiting (2), we can determine the relation between the thermistor operating point and its dynamic characteristics:

$$K(T) = \frac{\Delta(V_T(T))}{\Delta I(T)}. \quad (3)$$

For a semiconductor thermistor it can be written:

$$K(T) = \frac{\Delta P_T}{\Delta T} = \frac{\Delta P_T}{\Delta R} \frac{\Delta R}{\Delta T} = -\alpha \frac{\Delta P_T}{\Delta R}, \quad \alpha = \frac{\Delta R}{\Delta T}, \quad \alpha \quad (4)$$

Using (4) and the relation $\Delta R = \Delta(V/I)$ in (3) it results that:
\[ K(T) = -\alpha I^2_T \frac{Z + R}{Z - R}, \quad Z = \frac{\Delta V_T}{\Delta T}, \quad R(T) = \frac{V_T}{I_T} . \]  

(5)

\( Z \) being the differential impedance on the I-V curve. Since from the first law of thermodynamic \( K(T) \) must be positive, it follows that, under a whatever condition, \( R \geq Z \) must be always satisfied. In addition, if the thermal conductance is large, or there is a good thermal contact, then \( Z \) tends to be close to \( R \), and the I-V curves become straight-lines.

Eq. (5) sets a relation between the thermistor current and its static, small signal (differential) characteristics.

A scheme for the small signal model of the electro-thermal effect is shown in Fig. 4 [14], [15]. Let’s first consider the feedback effect suppressed by connecting the (not present) virtual switch SW to the heat sink. We would expect that, as a response to a small input power \( P_i \), an open loop change of the temperature \( T \), \( T_{OL} \), results in:

\[ \Delta T_{OL} = \frac{\Delta P_i}{K + j\omega C} . \]  

and, consequently, a change is set also for the thermistor resistance \( R(T) \), \( \Delta R = -\alpha \Delta T \). The electrical power undergoes a change proportional to \( \Delta R \) that, in turn, is proportional to \( \Delta T_{OL} \): \( \Delta P_F = -\alpha \Delta T_{OL} \). When SW is connected to the heat sink this quantity is proportional to the open loop gain, \( LG(\omega) \), therefore:

\[ LG(\omega) = \frac{\Delta P_F}{\Delta P_i} = -\frac{\alpha A}{K + j\omega C} . \]  

(7)

By considering the virtual switch SW connected to the node at the temperature \( \Delta T \), the overall transfer function becomes:

\[ \Delta T = \frac{1}{K + j\omega C} \frac{1}{1 - LG(\omega)} \Delta P_i . \]  

As known for a feed-backed system having a dominant pole, the open loop time constant, \( C(T)/K(T) \) for the present case, is reduced by a factor proportional to the value of \( 1-LG(0)=1+\alpha A/K \).

The term \( A \) in (7) can be extracted from the electrical mesh of Fig. 4 (it has to be remarked that, when \( V_{BIAS} \) does not change, the operating point jumps from one curve to another in response to \( \Delta P_i \) in Fig. 2):

\[ A = \frac{\Delta P_{EL}}{\Delta R} = \frac{Z_L - R}{Z_L + R} \frac{I^2}{I}, \quad I = \frac{V_{BIAS}}{Z_L + R} . \]  

(9)

It is interesting to observe that the feedback can result regenerative and the detector may break into oscillation at any frequency for which \( |Z_L| \) results less than \( R \). Or the system transfer function may have two or more poles if \( Z_L \) is complex, i.e. as a typical case \( Z_L=R_\perp || C_L \), where \( C_L \) may be a parasitic shunting capacitance.

![Fig. 4: Electro-thermal model of a bolometer.](image)

We can also evaluate the expected dependence of \( Z \) on frequency, \( Z(\omega) \). If we apply a high frequency excitation to the bolometer, the heat capacity will respond with a thermal short circuit to the heat sink. Hence \( Z(\omega)=R(T) \) and, since \( Z(0)=Z \leq R(T) \), \( Z(\omega) \) is expected to increase with frequency, showing an inductive behavior. The mathematical interpretation of this can be made considering a small variation of the bias voltage \( V_{BIAS} \), \( \Delta V_{BIAS} \), in Fig. 4. From the output
In our experiment the operating temperature is about 9.7 mK, starting from an heat sink temperature of about 7 mK, the bias current \( I_T \) is 20 pA and \( R_T(T) \) is about 100 MΩ. \( A_{PGA} \) is 7500 V/V, \( g_m \) 4 μA/V and \( R_h \) 50 KΩ. The sensitivity α therefore results about 10^{11} Ω/K (\( T_0 = 3.3 \) K), while the thermal conductance is 14 μK/W (\( K_T(T) = 1.56 \times 10^{-3} T \) K/W for the copper strips used in CUORICINO [16]). The quantity \( K_T/T \) in (15) is about 80 nV. This means that the bias of the thermistor is forced to be very close to \( V_{OFF} \), the chosen set point, apart from (15), \( Z_T \) becomes negligible. In the simulations of Fig. 6 it is shown how the ratio \( Z_T/R_T \) assumes small values of about 0.0092 at the operating point. It is possible to see that the I-V curves show a linear behaviour till the set point \( V_{OFF} \), of about 2.2 mV, is reached. This happens because if the current given to the thermistor develops a voltage smaller than \( V_{OFF} \) the feedback would try, unrealistically, to lower the thermistor bias and the thermistor has the constant value it should have at that heat sink temperature.
The above described operation is allowed by the block g_m of Fig. 5, whose circuit diagram is shown in Fig. 7. Two current generators A_G1 and A_G2 convert the differential input voltage, amplified of a factor 2, in a current given to the heater R_h. As a consequence the value of g_m=I_h/(VA-VB) results equal to 2/R_1, where R_1 has been chosen equal to 10R_h. The circuit has been designed such that the current can be given to the heater only in one sense. This prevents any regenerative effect that can take place when a too small value of bias current is given to the thermistor, or the thermistor operating point is in the linear region of Fig. 6. Diode D_N and resistor R_N are added to limit a possible large current given to the heater R_h. This can heat the system to much, with a consequent long recovering time. Com short circuits R_h if the thermistor operating point is in the linear region of Fig. 6. The inclusion of the comparator Com was found very useful. Sometimes it happens that when the loop is closed the first negative excursion of the input of AG1.

The circuit that generates g_m is the only part of the feedback added to the configuration of a standard front-end circuit used in CUORICINO. It has to be remarked that the operating point of thermistor R_T can be chosen by simply exploiting the offset correcting circuit that equips any other channel. The correction is remotely made and a binary code is stored. This way if, for any reason, the system must be restarted the offset binary code can be reused, allowing to get the same final stabilized temperature for the frame and the detectors.

Eq. (15) accounts for the static behaviour of the system. An estimation of the dynamic performance can be evaluated. First we have to calculate the quantity A of (7) that is:

\[
A = \frac{\Delta P_{EL}}{\Delta R} = 2(V_T - V_{OFF})A_{PGAG}g_m^2\frac{R_L}{R_L + R_T}I_T - \frac{R_L}{R_L + R_T}Z_T \frac{K_F(T)}{R_T}. \tag{17}
\]

where use has been made of (15).

Now suppose that an input disturbing power, \(\Delta P_n\), tries to heat the frame. From (8) we have:

\[
\Delta T_n = \frac{1}{j_{0}C_F + K_F Z_T} + \frac{1}{R_L + R_T} \frac{\Delta P_n}{Z_T}. \tag{18}
\]

The final expression is very simple. The feedback has the effect to reduce the thermal constant and attenuate the temperature change consequent to a noisy input power by a factor of \(Z_T/R_T\). In the case of CUORICINO this factor was calculated in the previous section to be about 0.009. The heat capacity of the oxygen free copper frame of CUORICINO is \(C_F(T)=1.2 \times 10^5 \times 12000 T\), or about 1.4 mJ/K. The open loop time constant is \(C_F/K_F \approx 100\) sec. The feed-backed time constant is reduced to less than about 1 sec. The same applies also for the amount of temperature change.

There is a latter important aspect concerning the adopted system. From (15) it is possible to verify that the stabilized temperature may drift with R_h and/or V_OFF and/or V_BIAS. Nevertheless these 3 elements are of the same type of those used to operate any detector of the array. The consequence is that the stabilization system, on the average, compensates not only for the drift of the heat sink temperature, but also for the drift coming from these other possible contributing elements.
III. EXPERIMENTAL RESULTS

To reach the cryogenic temperature of about 7 mK necessary to run CUORICINO we use a dilution refrigerator. A gas mixture composed of $^3$He-$^4$He is forced to circulate between room temperature and the cold finger, to which the detector frame is thermally connected with 2 copper strips. While circulating from room temperature down to the lower temperature the mixture is cooled by the thermal contact with various thermal stages. The described process and the properties of the $^3$He-$^4$He, a Fermions-Bose gas, allow to reach the very low expected temperatures.

The first 2 stages at the higher temperatures, the main responsible for the detector drift, are the main bath and the 1 K pot. The main bath is the Liquid He, LHe, reservoir at 4.2 K. The 1 K pot is a vessel that is filled with liquid from the main bath and is continuously pumped such that its temperature lowers to 1.2 K. To maintain the level in the 1 K pot constant an equilibrium must be found between the filling and the pumping efficiency.

To compensate the LHe consumption we have used 2 methods. 1) The He gas evaporated from LHe in the main bath is driven to a liquefier to produce LHe that the liquefier itself injects back in the main bath; 2) a periodic refilling of the main bath is made by a human intervention. We used method 1) in the first part of our experiment, but after some mechanical problems we decided to use method 2), so removing the liquefier.

At the beginning of the CUORICINO run the stabilizing system was not in use. In Fig. 8 we can see the baseline drift of 5 detector channels, chosen to represent the typical observed behaviour, during few days. Since the liquefier had not full efficiency, the level of the main bath lowered by about 2.2 %/day. As a consequence the baseline of the detectors changes accordingly. Due to the good thermal sensitivity of our bolometers, this drift spreads between 50 keV/day to more than 150 keV/day. In the period considered here the filling level of the 1K Pot was very stable, about -0.6 %/day, see Fig. 9. The conversion in keV of the baseline drift corresponds to about 300 nK/keV and about 600 nK/keV of detector temperature change, depending on the crystal in the array, $(5 \times 5 \times 5$ cm$^3$ or $3 \times 3 \times 6$ cm$^3$). From Fig. 8 we have that the temperature drift is close to 15 µK/day to 45 µK/day for the larger detectors.

Things became completely different as soon as the stabilization system was introduced. In Fig. 10 the drift of the same set of detectors is shown during a similar time period. The baseline drift is harder to be detected. As an upper limit we quote it between -0.02 keV/day (6 nK/day), for the best situation, and -0.84 keV/day (250 nK/day) at worst. If we consider the fact that in the same period the main bath level dropped-out by about -0.93 %/day, the reduction of the drift was never less than a factor of 70 and even more than a factor of 200 (2000 for the very best case) with respect to those of the pre-stabilization period.

It has to be remarked that although while stabilization was used the main bath level had small variations, the 1k Pot emptied daily, Fig. 11. This is the reason why the main bath level of Fig. 10 is not a straight line. It undergone to small periodic changes caused by the complete filling of the 1k Pot. The stabilization system was able to reject also this effect.

![Fig. 8: Drift of 5 channels, the labels indicate their convention name, of CUORICINO before system stabilization, left axis, the minimum drift is channel B54, 55 keV/day, maximum drift is channel B45, 173 keV/day.](image1)

![Fig. 9: 1K Pot level changes about -0.6 %/Day during the period shown in Fig. 8.](image2)

A probe of the efficiency of the stabilization system is the present situation in which there is a complete refill of the main bath every two days. As it can be seen in Fig. 12, where another set of detectors is shown for generality, the average drift does not change, during two successive fillings of the main bath, with respect to the previous filling method also in this very extreme case. Fig. 13 shows a longer measurements period, in which the main bath is completely filled many times. Fig. 14 shows the level of the 1K Pot during a similar time period of that of Fig. 13. Although it was refilled asynchronously with respect to the main bath, no effects are
visible in the baseline shift. This result shows that there is a very high rejection of the drift of the refrigerating system by the use of the implemented instrument.

The large insensitivity of the detector baseline to the main bath level is the more remarkable result obtained. It allows the periodic complete refilling of the main bath otherwise not possible without the stabilization system.

It has to be remarked that the quoted figure is not limited by the developed instrument, but from the sensitivity of the adopted sensor elements. Since our instrument exploit the same kind of sensor as those of the detector array, it is able to handle cases in which more sensitivity is provided by the detecting method.

![Figure 10: Baseline of the selected channels, the labels indicate their convention name, after stabilization. An energy offset of 300 keV has been added to the 4 upper channels to guide the eyes. The right axis is the liquid level inside the main bath. The smaller drift is from channel B13, -0.02 keV/day, the larger from B42, -0.84 keV/day. The main bath level drop was about -0.94 %/day.](image)

IV. CONCLUSIONS

A very simple circuit solution has been developed to implement the temperature stabilization of an array of large mass bolometric detectors. The circuit exploits the front-end to perform the task. Adding a very simple transconductance amplifier the final drift was reduced at least a factor of 70 with respect to the open loop condition. Many channels had even better improvement, of a factor 200 and more. The final figure of merit is a drift always better than 0.8 keV/day, or about 250 mK/day, for a full excursion of the level of the refrigerating liquid in the main reservoir, this figure being limited by the sensitivity of the thermal sensor used in the array.

Since the stabilization system bases its operation exploiting the same kind of equipment of any other detector of the array, the further figure of merit is the rejection of the room temperature drift on the circuit devices that compose the front-end.

Thank to the use of the front-end, the sensitive element can be chosen similar to any other bolometer of the array, obtaining the same level of sensitivity in the temperature stabilization.

The developed instrument was introduced in the CUORICINO experiment in January 2004 and is currently in use since then.

The modelling of the stabilization system has been done by reviewing the theory of operation of a bolometric system using the concept of a feedback network.

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VI. REFERENCES


Fig. 11: 1k Pot level. A refill was necessary any about 1.5 Days in the same period as that of Fig. 10.

Fig. 12: The residual drift of a few detector channels, the labels indicate their convention name, without the presence of the liquefier and limited to two days, the period between the successive refill of the He Main Bath. The worst drift is 0.9 keV/day. An energy offset of 500 keV has been added to the 4 upper channels to guide the eyes.

Fig. 13: The residual drift of a few detector channels, the labels indicate their convention name, without the presence of the liquefier and with refilling of the He Main Bath any 2 Days. The observed drift is similar to that shown in Fig. 12. An energy offset of 500 keV has been added to the 4 upper channels to guide the eyes.

Fig. 14: The 1k Pot level during the same period of time of Fig. 13.