SLEW-RATE ENHANCEMENT TECHNIQUES TO BE USED WITH SILICON CALORIMETERS CHARGE SENSITIVE PREAMPLIFIERS

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Circuit techniques for improving the slew-rate performance of a folded-cascode charge sensitive preamplifier to be used in silicon calorimeters are proposed. The solution consists of an additional circuit, active only during the slewing period. It operates by enhancing the amount of the current steered to the output capacitor or with a frequency compensation which depends on the signal amplitude. The proposed solutions require negligible extra bias power and small additional area. The slew-rate is enhanced without changing the small signal response and the noise performance.

Introduction: Charge sensitive preamplifiers (CSP) are fundamental blocks in silicon calorimeter applications [1]. They process the detector signal which is composed of narrow current pulses with always the same polarity, but with different amplitude. The preamplifiers operate in the inverting configuration shown in Fig. 1. The resulting CSP output is a positive step voltage with a slow decay time-constant defined by \( R_L C_F \). The classical preamplifier configuration [1] is the folded-cascode, shown in Fig. 1, which offers large bandwidth, high output swing and low noise performance.

![Fig. 1 CSP configuration with folded cascode structure](image-url)

The high rate of incoming events forces analysis of the signal for a short time (<20ns). As a consequence the main noise contribution is due to series noise. In this case a bipolar input device has advantages over a FET device because of its larger transconductance for the same current.

There are three key performance parameters of the preamplifiers to be used with the new generation of silicon detectors at LHC: very large slew-rate (more than 600 V/\( \mu \)s) to allow an acquisition time of less than 10 ns for output signal up to 5 V amplitude, low noise and low power consumption due to the large number of such preamplifiers to be used in the calorimeters. To achieve a low collector shot noise a large current in Q1 (\( I_{Q1} \)) is required, resulting in a large \( I_{Q2} \).

For the same reason the current in Q3 \( I_{Q3} \) cannot be too low to reduce reflect back noise contribution. To ensure stability, a large compensation capacitance \( C_1 \) is required. Due to these three contrasting requirements there is a trade off between preamplifier noise (requiring large \( C_1 \) and its maximum slew rate (requiring small \( C_1 \)).

This Letter presents circuit solutions which achieve a slew-rate enhancement without changing the small signal response and therefore the noise performance. During the slewing period the new circuits allow an increase in the output current or a decrease in the loading capacitance. The proposed solutions compare favorably to previous ones [2, 3] in terms of simplicity, area and power.

Slew-rate enhancement techniques: In the classical circuit of Fig. 1, transistor Q1 is designed to reduce its input series resistance \( R_W \), a source of series noise. In addition, to maintain low the series noise coming from the collector shot noise \((4kT/\Omega_0)\), the bias current of Q1 must be in the mA range. To achieve a suitable small-signal gain-bandwidth product with a compensation capacitance \( C_1 \) as small as possible, the input-to-output transconductance must be degraded by operating Q3 with a small bias current, so increasing its input impedance with respect to the resistor \( R_L \).

During a large positive step at the high-impedance node the capacitance \( C_1 \) is charged with the current subtracted from Q1, which steers less current during the transient. The maximum rate of change is obtained when Q1 cuts-off, so the slew-rate is limited by \( I_{Q1}/C_1 \). A larger slew-rate is obtained by increasing \( I_{Q1} \), keeping the same \( C_1 \). This, however, serves to degrade further the input-to-output trans- conductance, reducing \( I_{Q1} \). This process cannot be carried on forever since the input referred noise contribution of Q3 would become unacceptable.

To enhance the maximum slew-rate above \( I_{Q1}/C_1 \) two approaches are suggested (which could be combined in the same CSP). First, for a given \( C_1 \), during the slewing period extra current can be provided at the output in addition to \( I_{Q1} \). Second, for a given current \( I_{Q1} \), during the slewing period the compensation capacitance \( C_1 \) can be reduced.

Fig. 2 shows a solution based on the first approach. Choosing \( I_{Q2} = N \cdot I_{QSR1} \) (with proper transistor area ratio \( Q1/QSR1 = N \)) and \( RSR = 2N \cdot R_L \), \( V_{Q2} - V_R = -I_{QSR} \cdot R_L \), results with \( I_{QSR} \) designed to be larger than 0.5 \( V_0 \). In this way, in quiescent condition QSR3 and QSR4 are cutoff. During the slewing period Q1 and QSR1 tend to cut-off, node B rises toward the power supply, QSR3 and QSR4 start to conduct delivering high current to the output node. In this way assuming \( \beta \) to be the current gain, the slew-rate current \( I_{QSR} \) is enhanced up to

\[
I_{QSR1} = I_{Q1} + I_{QSR2} = I_{Q1} (1 + \frac{\beta}{2N})
\]

(1)


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Fig. 3 illustrates a solution based on the second approach. The circuit reduces the effect of the small signal compensation \( C_{pl} \) on the large swing response. If the output voltage evolution satisfies the condition \( (dV_2/dt < I_q/C_{pl}) \), \( C_{pl} \) has negligible effect. When \( (dV_2/dt > I_q/C_{pl}) \), node \( C \) prevents a very high-impedance in series to \( C_{pl} \), which has negligible effect.

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Simulated performance: The proposed circuits have been simulated assuming a 2 \( \mu \)m BiCMOS technology (called HF2CMOS and developed by SGS-Thomson). Design parameters are \( I_{O1} = 2 \) mA, \( RL = 500 \Omega \), \( V_{DD} = 11 \) V. The step response for small (100 mV) and large (5 V) output signal are shown in Figs. 4 and 5, respectively. Line 1 refers to the circuit without improvement \( (C_p = 5 \) pF\). Line 2 refers to the circuit of Fig. 2 with \( N = 4 \) \( (C_p = 5 \) pF\). Line 3 refers to the circuit of Fig. 3 with \( C_p = 6 \) pF, \( C_{pl} = 1 \) pF. No difference is present for small output signal. For large output signal the slew rate is about 310 V/\( \mu \)s for the standard solution, whereas it is increased to greater than 1000 V/\( \mu \)s for both the improved solutions.

Fig. 3 Second slew-rate enhancement scheme

Fig. 4 Step performance for small output signal amplitude (100 mV)

Fig. 5 Step performance for large output signal amplitude (5 V)

Conclusions: Very simple slew-rate enhancement techniques have been proposed. The extra hardware cost is minimal, and negligible extra power or bias circuitry is required during the standby operation condition. The resulting performance is a slew rate higher than 980 V/\( \mu \)s. This technique has been developed to be applied in a high-performance charge sensitive preamplifier for silicon calorimeters at LHC.

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References

INHERENT PATTERN JITTER OF STM-64 FORMAT SIGNAL AND A REDUCTION METHOD

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Introduction: Synchronous digital hierarchy (SDH) is an international standard that defines a new digital hierarchy for synchronous optical transmission and a frame structure for multiplexing digital traffic. In the synchronous transport module level \( N \) (STM-N) signal, \( A_1 \) ('1110101', mark density 3/4) and \( A_2 \) ('0010100', mark density 1/4) of the section overhead (SOH) bytes continue for 3N bytes (15411 s). In addition, \( C_1 \) (channel numbers) and the '1010 ...' alternate bytes, which are for national use, also continue for 51 s and 103 s, respectively. When level \( N \) is 64 (equivalent to 9.95328 Gbit/s), the lengths of the \( A_1 \), \( A_2 \), \( C_1 \) and '1010 ...' bytes become longer than the time constant of a practical timing tank \( (t = 2Q/\omega_0 = 32 \mu s \) at \( Q = 1000 \)\). Therefore, DC-level fluctuation of the incoming data stream and the output power variation of the timing tank cause phase deviation in the first row of the SOH. This phase deviation generates the inherent pattern jitter of the STM-64 format signal.

We have proposed a 10 Gbit/s timing recovery circuit using two cascaded differentiators as the jitter suppression equalizer [1]. This Letter describes the mechanism leading to increased pattern jitter in the first row of the SOH and demonstrates its reduction using this circuit.

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References