Voltage-Sensitive Differential Input Preamplifier
with Outstanding Noise Performances(*)

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Abstract. A voltage-sensitive, differential input preamplifier is here described. It employs recently developed junction field-effect transistors featuring particularly good noise characteristics. The use of these active devices, along with a new design idea which helps to keep the thermal noise from external resistors low, result in outstanding noise performances.

1. PREAMPLIFIER CONFIGURATION

The differential–input preamplifier of figure 1 is a balanced structure obtained by coupling through the resistor \( R_1 \) two identical feedback loops \((J_1, T_3, T_2)\) and \((J'_1, T'_3, T'_2)\). Each loop consists of a field-effect transistor, \( J_1 (J'_1) \) to the gate of which the input signal is applied, followed by a current amplifier \( T_3, T'_3 (T'_3, T'_2) \). The feedback is returned to the source of \( J_1 (J'_1) \).

Under the hypothesis of infinite loop gain for the feedback amplifiers, a difference input voltage \( v_{G1} - v_{G1}' \) would result in a difference between the source voltages

\[ v_{S1}' - v_{S1} = v_{G1}' - v_{G1} \]

A current equal to \((v_{G1}' - v_{G1})/R_1\) flows consequently across \( R_1 \) and the \( R_2 \) resistors of both amplifiers. The resulting voltage difference at the input of \( A \) is, accordingly:

\[ v_{C5}' - v_{C5} = 2R_2 \frac{v_{G1}' - v_{G1}}{R_1} + v_{G1}' - v_{G1} \]

The differential voltage gain of the amplifier is therefore:

\[ A \cdot \frac{v_{C5} - v_{C5}'}{v_{G1} - v_{G1}'} = A \left( 2 \frac{R_2}{R_1} + 1 \right) \]

(1)

The main noise sources in the preamplifier are:

- thermal noise in the channels of \( J_1, J'_1 \)
- \( 1/f \) noise associated with drain currents of \( J_1, J'_1 \)
- thermal noise in the feedback resistors \( R_1, R_2 \)
- shot noise in the leakage currents of \( J_1 (J'_1) \) gates

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Fig. 1 – Oversimplified configuration of the differential input preamplifier.

If the shot noise in the gate leakage currents as well as the coupling effect of the thermal noise in the channel to the gate through the channel gate capacitance are
neglected [1] and $R_2 > R_1$, as required by the need of achieving a substantial gain, the noise behaviour of the preamplifier can be described by a single noise voltage source in series with the gate lead of either $J_1$ or $J'_1$ with the following spectral power density:

$$
\frac{d\overline{e^2}}{df} = 4kT \cdot \frac{0.7}{g_m} + 4kT \cdot \frac{0.7}{g_m} + 4kT \cdot R_1 \cdot \frac{A_{J_1}}{f^2} + \frac{A_{J'_2}}{f^2} + \frac{A_{J'_2}}{f^2} + \frac{A_{J'_2}}{f^2}
$$

(2)

In equation (2) the first two terms account for the thermal noise in the channel of $J_1$, $J'_1$, $k$ is the Boltzmann’s constant and $T$ the absolute temperature [2]. The third term accounts for the thermal noise in $R_1$, which is the dominant contribution from thermal noise due to source coupling and feedback resistors. The last four terms in eq. (2) describe the $1/f$ noise [3], [4] noise in the drain currents of $J_1$, $J'_1$. The discussed noise representation is actually a simplified one which is valid as long as the drain-to-gate and gate-to-source capacitances of $J_1$, $J'_1$ are neglected.

The preamplifier realization described here employs field effect transistors of very recent design, featuring $g_m$ value of 200 mA/V at a standing $I_D$ of 20 mA [5]. The $0.7/g_m$ terms in equation (2) are as small as 3.5 $\Omega$.

In order to make the thermal noise contribution due to $R_1$ negligible, $R_1$ should be chosen below 1 $\Omega$.

Such a low valued $R_1$ makes the dc coupling between the two sections ($J_1$, $J'_1$, $J_1$, $J'_1$) somewhat critical. Any differential mismatch or offset $\Delta(V_{G_{1}} - V_{G_0})$ would result, if the currents $ID_1$, $ID_0$, $IR_1$ of both sections are kept constant, in a differential unbalance $\Delta(I_{C_5} - I_{CS})$ given by:

$$
\Delta(I_{C_5} - I_{CS}) = 2 \cdot \frac{(V'_{G_1} - V_{G_0})}{R_1}
$$

Such an unbalance may impair the stability or even the feasibility of dc coupling between the two sections.

A solution which balances the dc operating point of the preamplifier, regardless of any possible mismatch in the static characteristics of $J_1$, $J'_1$ is shown in figure 2.

Stabilization of dc operating condition is achieved with an additional feedback loop consisting of the integrator $I$ and transconductance amplifier $G$.

The integrator senses the voltage difference across $R_1$ and its output voltage $v_{i1}$, through the transconductance amplifier $G$, controls the correcting drain current of $J_1$.

The transfer function between the input difference voltage and the output difference $v_{C_{5}} - v_{CS}$ becomes, taking into account the dc stabilizing feedback:

$$
\frac{v_{C_{5}}(s) - v_{CS}(s)}{v_{G_{1}}(s) - v_{G_{0}}(s)} = \left(1 + \frac{2R_2}{R_1}\right) \cdot \frac{sRC}{sRC + \frac{g}{g_m}}
$$

(3)

where $s$ is Laplace complex frequency.

In Laplace transform domain, the relationship between the input difference voltage and the difference $I_{C_5} - I_{CS}$ is given by:

$$
\frac{i_{C_5}(s) - i_{CS}(s)}{v_{G_{1}}(s) - v_{G_{0}}(s)} = \frac{2}{R_1} \cdot \frac{sRC}{sRC + \frac{g}{g_m}}
$$

(4)

By virtue of the dc stabilizing feedback loop, both transfer functions (3) and (4) are of the approximate differentiator type, with a real pole and a zero at $s = 0$. Consequently, slow variations in $v_{G_{1}} - v_{G_{0}}$, like thermal and long term differential drifts do not affect the current and voltage dc balance in the circuit.

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**Fig. 2 – Voltage sensitive differential input preamplifier with dc condition stabilizing loop.** Black letters denote the stationary circuit variables, while small letters refer to signal components.

The detailed circuit diagram of the preamplifier is shown in figure 3.

The two preamplifier sections consists of the junction field-effect transistors $J_1$, $J'_1$ and of the bipolar transistors $T_2$, $T_3$, $T_4$, $T_5$, $T'_3$, $T'_4$, $T'_5$.

The components $J_1$, $T_3$, $T_5$ and $J'_1$, $T'_3$, $T'_5$ implement the same functions of the corresponding components in the circuit diagram of figure 1. The emitter followers $T_3$, $T'_4$ introduced between $T_3$ and $T_5$ and $T'_3$ and $T'_4$ in the actual circuit have the purpose of increasing the open-loop gain of the individual amplifier sections. The emitter followers $T_2$, $T'_2$ that sense the voltage on the source of $J_1$, $J'_1$ make a two-fold bootstrapping action possible.
The former feeds, through $T_2$, $T_3$ and $T'_2$, $T'_3$, the source voltages of $J_1$, $J'_1$ back to their drains, thereby keeping the voltage across the gate-to-drain capacitances constant. This results in a reduced capacitive component at the preamplifier inputs. The latter bootstrapping action aims at keeping the voltage drop across the $51\,\Omega$ resistors on the drains of $J_1$, $J'_1$ constant, thereby avoiding possible dynamic reductions in the resistive loads on $J_1$, $J'_1$ drains.

The dc conditions stabilizing network, as in the simplified diagram of figure 2 senses the voltage across $R_1$ with the differential integrator $I$, whose output voltage is employed to correct the drain current in $J_1$ until the voltage across $R_1$ approaches zero. The actual implementation of the dc stabilizing network slightly differs from the simplified model of figure 2, as the output of $I$ is applied to the base of $T_3$ through the 12 kΩ resistor.

Being the dc current through resistor $R_1$ zero, the biasing current of $J_1$ ($J'_1$), set to $20$ mA, flows across the $R_2$ resistors.

Since both inputs are at ground level through the $100 \, \text{MΩ}$ gate biasing resistors, both sources are slightly positive.

The biasing current determines a drop of approximately 4 Volt across $R_2$ making the collector of $T_2$ ($T'_2$) sufficiently negative to enable a total peak to peak swing of 8 V at these points.

The output amplifier $A$, a difference feedback configuration, introduces a further gain of 6 on the voltage difference $v_{c5} - v_{c2}$ and delivers the output signal to the load.

2. PREAMPLIFIER PERFORMANCES

In the design of the preamplifier, emphasis was put on the achievement of outstanding noise performances. Attention was accordingly concentrated on the choice of $J_1$, $J'_1$ as well as on keeping the thermal noise contribution from external feedback resistors as small as possible.

The input field-effect transistors are special units developed by INTERFET CORPORATION for INFN-Milano and intended for calorimetry applications in the experiment ICARUS [2]. These FET's have a pinch-off voltage below 1V and feature a $g_m/I_D$ ratio of 10 at values of $I_D$ around 20 mA. At these $I_D$ values, the total input capacitance $C_{GS} + C_{GD}$ ranges between 400 and 500 pF.

The thermal noise contribution due to $R_1$ can be made negligible by making $R_1$ equal to 1 Ω or smaller, which can be done without impairing the dc circuit balance by virtue of the dc stabilizing loop.

The circuit of figure 3 has a midband differential gain of 67 dB. The magnitude of the differential gain drops with increasing frequency as shown in figure 4.

At low frequencies where the loop aiming at stabilizing the dc operating condition becomes active, the magnitude and the phase of the gain have the frequency dependences shown in figure 5.

The actual network employed to stabilize the dc operating condition has, apparent in figure 3, besides the pure integrator $I$, an approximate integrator determined by the capacitors shunting the base of $T_2$ to ground. It affects, therefore, the gain in the low frequency region with a zero at $\omega = 0$, one more real
zero and two poles that, with the values of the circuit parameters employed, are complex.

The very good rejection of the differential input preamplifier for common-mode signals are put into evidence by the diagrams of figure 6, describing respectively the magnitude of the CMRR as a function of frequency and the phase shift of the transmission of common-mode signals as a function of frequency.

As shown in figure 6 the magnitude of the common-mode rejection ratio approaches 100 dB as the frequency ranges between a few Hz and 100 kHz.

The excellent result regarding the CMRR is obtained by using a balanced input configuration, in which special attention was put in making both channels identical. The reduction of drain to gate effective capacitances due to the action of \( T_2, T_3 \) extends the frequency range in which the CMRR is higher than 100 dB up to 100 kHz. The operational amplifier following the first stage, a Harris HA–2625, includes in its feedback network an adjustment potentiometer which compensates further unbalance of channels' gain. The use of a carefully designed printed circuit board proved to be extremely useful in getting identical channel characteristic.

The very good noise performances of the preamplifier are described by the plots of figures 7, 8 and 9.
representing respectively the spectral power densities referred to the input in the white noise region, figure 7, and in the low frequency part of the spectrum, figures 8 and 9.

As a result of the large $g_m$ featured by $J_1$, $J'_1$, as well as of the small value (1 Ω) chosen for $R_1$, the spectral power density in the white noise region turns out to be as small as 410 pV/$\sqrt{\text{Hz}}$.

As shown in figure 8, the preamplifier behaves well also from the point of view of low frequency noise. An input spectral density of 1.73 nV/$\sqrt{\text{Hz}}$ has been measured at a frequency of 15 Hz.

3. CONCLUSIONS

The voltage-sensitive differential input preamplifier described in this paper features a large bandwidth and a good capability in rejecting common-mode deterministic disturbances.

It has excellent stochastic noise performances, resulting from special, large $g_m$ input field-effect transistors of very recent design and from a circuit conception aiming at keeping the thermal noise from external feedback resistors at negligible small values.

These combined characteristics make the preamplifier suitable to cover a broad range of scientific applications.

In particular this circuit was used in the amplification of the pulses coming from a cryogenic detector currently under development by the Milano group [6].

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REFERENCES


