The Preamplifier for CUORE, an Array of Large Mass Bolometers

C. Arnaboldi, X. Liu, G. Pessina

Abstract—We present the preamplifier for the readout of the 988 large mass bolometers of the CUORE experiment. Each bolometer is based on a 750 g TeO₂ crystal on which a Nuclear Transmutation Doped Ge thermistor, NTD Ge, is glued, in good thermal contact. To read out the detectors we have developed a differential voltage sensitive preamplifier based on a well selected and properly biased input JFET and by a circuit solution based on operational amplifiers. The developed preamplifier has a very small parallel noise, 0.094 fA/√Hz, and a small voltage noise of 4.9 nV/√Hz at 1 Hz and white noise of 3 nV/√Hz. To allow the DC readout of bolometric detectors, the preamplifier has added a circuit for the compensation of the detector bias and the offset of the input JFET pair. An additional compensation circuit allows to minimize the voltage thermal drift. The common mode rejection ratio is digitally adjustable. DC coupling, low noise, small thermal drift and CMRR are stringent requirements of the CUORE experiment. We will describe in detail the circuit solutions and the selection criteria for devices used.

Index Terms—Electronics for bolometric detectors, low noise, low noise amplifier, low thermal drift, programmable system.

I. INTRODUCTION

Bolometric detectors are instruments that allow to study rare nuclear processes with high degree of precision and a great flexibility in the material which form the sensitive part of the detector. For exploiting this possibility it is in preparation the CUORE experiment, an array of 988 large mass bolometers, 750 g each, for the study of the double beta decay of Te [1]. Each bolometer is formed with a TeO₂ crystal on which a Nuclear Transmutation Doped Ge thermistor, NTD Ge, is glued in good thermal contact. The TeO₂ crystal, after having absorbed the impinging particle, is subjected to a temperature increase, while the NTD Ge thermistor converts this temperature increase to an electrical signal [2] having a frequency bandwidth of a few Hz. The operating temperature of such a system is around 10 mK.

To read out the detectors we have developed a differential voltage sensitive preamplifier based on a selected and properly biased input JFET [3] and on a circuit solution based on operational amplifiers. The core of the preamplifier is an improved version of the one developed for CUORICINO [4], an array of 62 detectors used to study the feasibility of CUORE. The new preamplifier has at its input a JFET pair, SNJ132287, operated with a V_DS of 0.64 V, to optimize the device dynamic characteristics and to minimize the input current for obtaining a small parallel noise [3]. The expected input current at 40 °C is 55 fA and the parallel noise, in the case of differential biasing network, is 0.094 fA/√Hz.

In the following sections the preamplifier will be described and its experimental results will be shown.

II. THE DETECTOR READOUT

For the readout of the bolometers of CUORE a room temperature readout system has been chosen. In Fig. 1 it is reported the conceptual readout scheme. The thermistor glued on the absorbing crystal located in the colder part of the refrigerating system (the cryostat) is connected to the room temperature electronics by means of a dedicated link [5]. The readout link serves also for the thermistor biasing, through the two room temperature operated load resistors R_L and a differential voltage source V_{b1} and V_{b2}.

![Fig. 1. Conceptual scheme of the detector biasing and differential voltage readout.](image-url)

The thermistor is read with a room temperature operated fully differential voltage sensitive preamplifier based on a pair of JFET transistors accurately selected and characterized [3]. The fully differential configuration, with respect the single ended one, has a larger noise, but it allows the suppression of the disturbances coming from AC line ground loops and microphonism coming from the electrical connecting link, two sources of noise of great influence with large mass bolometers.
III. CIRCUIT DESCRIPTION

A. The preamplifier.

The new preamplifier is an improved version of the circuit developed for the COURICINO experiment [4]. It is a fully differential voltage sensitive preamplifiers (DVP) based on a pair of JFETs selected to have a small parallel noise contribution [3] and low series noise.

The simplified schematic of the DVP is shown in Fig. 2.

![Simplified diagram of the DVP with input stage and feedback network](image)

**Fig. 2. Simplified diagram of the DVP with input stage and feedback network into evidence.**

The two JFETs, like in the CUORICINO preamplifier, have the drains connected to the Operation Amplifier (OpAmp) based network, JFET Readout Network (JFRN), present inside the box of Fig. 2. The network provides to fix the drain voltage, to balance the drain currents and to drive the outputs.

Since the feedback forces the JFET Sources to follow the inputs, in first approximation, the gain of the preamplifier is \( GV = 1 + 2 \times RF/RST \), where \( RST \) is the total resistance between the two sources. In the CUORE preamplifier we added a resistor \( RS \) to allow, thanks to the mechanical relay \( S \), the selection of two different gains, 27 V/V with \( S \) open and 202 V/V with \( S \) closed. The lower gain 27 V/V, by extending the dynamic, is useful during the detector DC characterization phase, when large bias is given to the thermistor. In parallel to the \( S \) contact there is a 47 nF capacitor, not shown in the figure, that assures circuit stability at the lower gain.

In the CUORE preamplifier we have modified the current generator that bias the JFETs. In Fig. 2 it is modeled with the current generator \( I_B \) and the two new equivalent negative resistors \( R_F \). In Fig. 3 there is the detailed scheme of this block. The \( I_B \) node, corresponding to that common to the two resistors \( RS_1 \) of Fig. 2, is at the fixed current, 1.28 mA, thanks to a Howland current generator built with the two resistors \( R_B \) and the \( x2 \) gain block. In response to a common mode input signal in the two resistors \( RS_1 \) current is not expected to flow while the outputs must remain zero. From Fig. 2, if the two resistors \( -RF \) were missed, the current to resistors \( RF \) should be provided from the JFETs. The presence of resistors \( -RF \) avoid this, maintaining unaffected the bias of the JFETs. The model of resistors \( -RF \) of Fig. 2 is implemented by resistors \( R_F \) of Fig. 3, where we modified the Howland current generator. As an example a common mode input voltage change of 1 V, if we consider also other contributions that will be described later, generates a current change of about 150 µA, not negligible if compared with the JFET bias of 500 µA. It is very important to avoid changes in the JFET bias because the thermal calibration is otherwise affected.

In the CUORE JFRN we have used a new voltage translator that fix the JFET drain voltages in function of the common mode voltage of the JFET sources. The \( x2 \) gain stage used by the Howland current generator that bias the JFETs is now exploited also to force a current in the resistor \( RT \) of Fig. 4 developing a voltage drop of known value. Node \( V_D \) of Fig. 4 is read by the two current to voltage converters that determine the drain bias voltage of the two JFETs. Resistor \( R_D \) connected to the \( x2 \) gain block compensate the current change on the \( R_D \) connected to the reference voltage, \(+VREF\), fixing the current trough \( R_T \), forcing the \( V_D \) voltage change to be equal to the \( V_G \) one. Solving the network of Fig. 4 it results \( V_D = V_G + VREF/(2+R_D/R_T) \). The equation prove that \( V_D \) follow \( V_G \) with an offset proportional to \( +VREF\).
Fig. 4. Scheme of the voltage translator used to generate the JFET drains control voltage, V_D.

B. The offset and drift correction system.

As described in the previous section, the sources off the JFET are forced by the feedback to follow the inputs. This help the implementation of an output offset and drift correction system. The correction system we adopted, reported in Fig. 5, is based on a differential control voltage V_CD used to force in the sources currents of opposite polarity that the feedback of the preamplifier deviate in the feedback resistors R_F, producing a differential output voltage. V_CD is generated by a summing amplifier and an inverting stage. The summing amplifier of Fig. 5 adds the correction signals: the offset correction voltage, Offset CV, separated in the coarse and fine part and the drift correction signal, Drift CV, separated in the coarse and fine part. As for the R_F resistors other two resistors of value R_C are in the feedback of the tail current generator of Fig. 3. For the generation of the offset and drift control voltages, we explored two possible solution: one version of the preamplifier based on Digital to Analog Converter, DAC, the other one based on Digital Trimmer, DTRIM.

In the Digital DAC version of the preamplifier, the offset coarse control voltage is generated by an AD5415 by Analog Device (AD) a DAC converter that can be also operated in bipolar mode thanks to its additional feedback resistor.

In the DTRIM version, the drift corrector uses a digital trimmer AD5263 by AD and the offset corrector the digital trimmer AD5282 by AD and a silicon switch ADG1636 by AD for the polarity selection.

Both versions operate the same way with respect to their references. The offset correction has a stable and low noise bipolar reference ±5 V generated by a low noise and low drift power supply/reference generator [6]. The drift correction system exploit four Base-Collector junctions of the transistors BC857C-E6327 by Infineon, two of them biased above ground, and two below ground. This way a thermal voltage of about ±4 mV/°C is generated. The junctions are biased at 400 μA. We have used two junctions to increase the thermal signal/noise ratio. The collector diode of the selected bipolar transistor has a 1/f noise of 28 nV/√Hz @ 1 Hz and a white noise of 1.06 nV/√Hz when biased at 280 μA.

Fig. 5: Scheme of the circuit adopted to force an offset and thermal correction to the preamplifier.

C. The gain thermal compensation.

The measurement of the gain stability showed a drift larger than that foreseen from the feedback resistors R_S, R_S1 and R_F (mini-melf, 15 ppm/°C). The measured thermal drift of the gain has been demonstrated to be given by the presence of the finite value of the JFET output impedance (r_0), that introduce a term that has drift. The JFRN force the two J-Fet drain voltages and the drain currents to be equal. This makes the JFET Sources differential signal, V_SD, to follow the differential Gates signal, V_ID, with an attenuation factor of V_SD = (gm*r_0)/(1+gm*r_0) * V_ID. This attenuating factor has a thermal sensitivity of about -20 ppm/°C that contributes to the gain. To cancel it, see Fig. 6, we added in series to R_S a 220 Ω NTC resistor with a 5.1 Ω resistor in parallel to obtain the corrected level of attenuation, to add an opposite gain thermal contribution.
IV. THE REALIZED PREAMPLIFIERS

To test the two preamplifier topology, the DAC and the DTRIM we have prototyped both. The two versions are layout on a 4-layer Printed Circuit Board of 34×80 mm² populated on both side.

A. The DAC based preamplifier.

In Fig. 8 there is the DAC based version. At the top of the figure there are the inputs where cuts have been machined on the PCB, to increase the insulation between the inputs to minimize parasitic currents of surface origin (dust, assembling residual, etc). An 8051 microcontroller, P89LPC925, is at the bottom, close to the outputs. It controls and configures the preamplifier and it is remotely connected with \( \text{I}^{2}\text{C} \) bus serial link. The microcontroller may also change the state of the mechanical relay with two of its pins. The same pins of the \( \text{I}^{2}\text{C} \) bus can be used to program the microcontroller with the In-Circuit-Programming, ICP, protocol. An Electrically Erasable PROM, EEPROM, with serial communication protocol, used to store the preamplifier calibration data exploited to calculate and set the operating condition of the DACs and trimmers, is present close to the microcontroller. The microcontroller has an 8 bits ADC that we exploit to read the preamplifier positive output voltage, the output of the JFET biasing current generator and a connecting pin used to select the preamplifier device address on the I\(^2\)C control bus. In the offset correction procedure the readout of the positive output is useful to the preamplifier to know the detector bias. The output of the current generator is important to know the preamplifier common mode input voltage.
B. The trimmer based preamplifier.

The PCB of the trimmer version is similar to that of the DAC version. The configuration of the parameters, the selection of the mechanical relay state and the polarity of the offset corrector, are controlled by the two trimmer AD5263 and AD5282, since the microcontroller is not present in this solution. The AD5263 is a quadruple 8 bits digital trimmer that has available two digital outputs useful to change the state of the mechanical relay. The AD5282 is a double 8 bit trimmer with a digital output used by the silicon switch to select the polarity of the offset corrector. The two devices and an EEPROM useful to store the calibration parameters are controlled by the I²C bus of the front-end microcontroller.

V. EXPERIMENTAL RESULTS

A. The gain linearity.

We have measured the gain linearity of the preamplifier with a sine wave at 1 KHz. The measurements have been done comparing the input and output RMS voltage with the digital multimeter Keythley 2700. The measure shown a maximum non linearity of 0.002%, see Fig. 9, for an output signal from 100 mV to 5 V RMS.

![Fig. 9: Preamplifier linearity plot.](image)

B. The gain thermal stability.

As anticipated in the preamplifier description we have measured without the thermal compensation a stability of -23 ppm/°C. The thermal behavior of the gates to sources signal transfer function shown a thermal contribution of about -20 ppm/°C. The gates to sources gain thermal behavior indicate a gm*r0 of about 120 V/V with a corresponding thermal contribution of -1200 ppm/°C. After the introduction of the gain thermal compensation we obtained a thermal stability of few ppm/°C, see values of Table 1, due in part on the mismatch of the thermal behavior of the feedback network, in part by the spread of the thermal behavior of the JFETs.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Gain (V/V), 25°C</th>
<th>Gain drift (ppm/°C), 25°C to 45°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>201.93</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>202.00</td>
<td>-3</td>
</tr>
<tr>
<td>3</td>
<td>201.91</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>202.13</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>201.89</td>
<td>-1</td>
</tr>
<tr>
<td>6</td>
<td>201.94</td>
<td>-2</td>
</tr>
<tr>
<td>7</td>
<td>201.98</td>
<td>-1</td>
</tr>
</tbody>
</table>

Table 1: Measure of the gain and gain thermal behavior of the measured samples with the NTC compensation.

C. The CMRR.

To test the CMRR of the preamplifier, after correction, we have used a 50 Hz sine wave 2 Vpp common mode input signal. We have added at the preamplifier output an additional gain stage to have a total gain of 422 V/V. As Fig. 10 shows, the residual output signal is 5.06 mVpp, that correspond to a CMRR of 105 dB. Before correction, the preamplifier had already a quite good CMRR of about 95 dB. The dynamics of the compensation at the output of the set-up, was 65 mVpp. The best compensation is limited to 5.06 mVpp because the circuit cannot compensate the reactive components present in the circuit.

![Fig. 10: Measure of the CMRR of the compensated preamplifier.](image)

D. The input noise.

We report in Fig. 11 the input noise spectrum of the preamplifier, DAC version. To show also the noise contribution of the offset and drift correction system we report in Fig. 12 the noise of the preamplifier operating without the
correction system. As can be seen an almost negligible contribution is added. The noise contribution of the correction system of the DTRIM version is expected to be even smaller with respect to the DAC version, because the resistors of the digital trimmers are smaller than the ones of the DAC and because the use of the polarity selection in the offset corrector system avoid the amplification of the noise of the reference lines, as it happens with a bipolar DAC.

![Noise spectrum of the preamplifier operating with a small input DC bias.](image1)

**Fig. 11:** Noise spectrum of the preamplifier operating with a small input DC bias.

![Noise spectrum of the preamplifier operating without the offset and drift correction circuit.](image2)

**Fig. 12:** Noise spectrum of the preamplifier operating without the offset and drift correction circuit.

### E. The thermal stability.

The temperature calibration of the preamplifiers is based on an accurate characterization of their behavior with respect to the correctors codes and the environmental temperature. The device thermal characterization is done by a Matlab code that controls the environmental chamber that selects the working temperature, the preamplifiers to change the configuration of the correctors, a multimeter Keythley 2700 to measure the preamplifier outputs and the Keythley 7700 multiplexer card in the multimeter Keythley 2700 to generate two programmable voltages useful to force to the preamplifier, thanks to a 101 V/V attenuator, a differential voltage. The programmable voltage source is useful in the characterization of the offset corrector to avoid the output saturation when operating at large offset corrections and to simulate a detector bias to characterize the device operation at different bias conditions. To characterize the preamplifier in thermal equilibrium we do the measurements at tree different temperature, 10, 27 and 41 °C. At the tree temperatures with Matlab we scan all the possible set points, one at time. In Fig. 13 there is the measurement of the preamplifier output voltage sensitivity to the offset coarse corrector, with the drift corrector fixed, and in Fig. 14 the measurement of the drift coarse corrector, with the offset corrector fixed. From the measurements it is possible to observe that the JFET pair of the sample measured produce an output offset of -3.5 V equivalent to 17.3 mV at the input.

![Preamplifier output variation at different offset coarse set point at different temperatures.](image3)

**Fig. 13:** Preamplifier output variation at different offset coarse set point at different temperatures.

![Preamplifier output variation at different drift coarse set point at different temperatures.](image4)

**Fig. 14:** Preamplifier output variation at different drift coarse set point at different temperatures.

All the measurements allow the calculation of the coefficients of the polynomial model that describe the preamplifier behavior that is useful for the calculation of the optimal configuration of the correctors to allow the operation with a small overall thermal sensitivity.
To describe the thermal behavior of the preamplifier of Fig. 13 and Fig. 14 we report in Fig. 15 the measure of its operation at different input bias with the coefficients calculated by the polynomial model. The interpolations of the measure at different temperatures show an input thermal drift below 100 nV/°C at 27 °C.

![Graph showing output thermal drift of a preamplifier operation with polynomial equations for different biases.]

Fig. 15: Output thermal drift of a preamplifier operation with the configurations defined from the model.

ACKNOWLEDGMENT

We would like to thanks Carl Rosenfeld and Ray Edmond for their help in the prototyping of the preamplifiers and for the procurement of the components evaluated in the selection phase.

REFERENCES


